Scaleable Intelligent Video Server System

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[2] **CO** = Confidential (only for members of the consortium + EC); **RE** = Restricted to a stated circulation list (+ EC) *[replace this footnote with the list]*; **PP** = Restricted to other FP6 participants (+ EC); **PU** = Public

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1 DOCUMENT CONTROL

1.1 Change History

Issue 1.0 This is the first release of this document.

1.2 Changes Forecast

There are no further changes expected.

1.3 Terms and Abbreviations

BER	Bit Error Rate
BIST	Built in Self Test
ATB	Analogue Test Bus
FIFO	First In First Out
PLL	Phase Locked Loop
POR	Power On Reset
PRBS	Pseudo Random Bit Sequence
PSU	Power Supply Unit
Rx	Receiver
Tx	Transmitter

1.4 Related Documents

Doc Ref	Title
SIVSS 002075	SIVSS DoW rev1.pdf

2 INTRODUCTION

In order for production to be viable on the full TeraChannel chip set the Cronos testchip first needs to be verified and characterised. The NRE costs are such on a 0.18u process that satisfactory results of both functionality and performance are prerequisite to tapeout of the full chipset. It is the intention of the Test Chip test card and the test chip itself to be used as tools for evaluating the transceivers performance and operation. The Cronos test chip will be assembled onto the transceiver test card via either direct attachment or via a high speed fuzz button test socket. On the card all possible access points into the transceiver are available, along with a high portion of reprogrammable logic to drive, configure and test the chip. Detailed characterisation of the transceivers will be possible with this card.

The approach outlined in this document is in no way meant to be rigid. The testing procedure outlined is considered to be a best practice approach, taking the commissioning of the board and the chip through a logical flow. Initial testing will be possible on the board itself without the presence of the Cronos testchip. This will ensure minimum likelihood of board level bugs impeding the testing of the Cronos device.

Testing of the test chips will allow us to evaluate the following areas of the design for performance, functionality, and compliance with the specification.

1. Power up
2. Reset
3. Bandgap reference
4. Power supply noise
5. Clock quality
6. Status flags
7. Pll Lock and acquisition
8. Mode control
9. Link alignment
10. Tx Duty cycle error.
11. Rx Duty cycle error
12. Phase interpolator linearity
13. Phase interpolator step size
14. Bist functions
15. ATB
16. Loop-back Tx Rx
17. Sync characters
18. Transmission Jitter
19. Transmission Phase Noise
20. Via resonance effects
21. Amplitude Level settings
22. Pre-emphasis settings
23. BER analysis
24. Transmission distance
25. Behaviour in different interconnects
26. I/O cell characterisation

3 DEVICE TESTING

The initial testing of the testchip will consist of basic electrical and continuity tests. Based on past experience of test and analysis of transceiver devices the electrical environment must first be proven to be clean.

After the board testing stage has been completed the electrical environment should be in a sufficient state for power on testing of the testchip. To ensure that the board is environmentally clean enough to support testing of the testchip measurements of both voltage and current will be taken with the chip fitted and without the chip fitted.

In doing this we ensure that compensation can be made for any voltage drops due to the inclusion of the testchip. Corrections can be made at the board level if necessary.

3.1 Power up

The first most basic set of tests once the test board has been commissioned, is to ensure the devices isn't shorted out internally. A simple observation of the PSU current is sufficient to confirm if any such catastrophic event has occurred during manufacture

Once confidence has been established that the chip is not internally shorted a series of tests involving running up the chip from power up to power down should be ran. During the initial testing no clock source needs to be supplied to the chip. Once satisfactory power on behaviour is established the common block enables can be released, and a clock applied. This will allow the results of the common block power up, power down to be observed.

Likewise with transceiver units themselves a series of power up to power down tests should be performed to ensure satisfactory start up of the units. As with the common block testing of the enables during the power on tests should be performed, allowing for an initial current consumption figure to be taken.

3.2 Reset Testing.

Using the register interface via the FPGA the chip should be put into reset mode this will hold all the registers in a known state. To further test the reset the common block and the transceivers have to be cycled through a reset operation. In the first instance the common block reset will have been tested during the nPD testing. To further test the reset functions each transceiver should be put into running alignment then into reset. A noticeable change in both PSU current and transceiver output should be seen.

3.3 Band-gap Reference Testing

Testing of the band gap will consist of initially powering up the biasing circuits and de-asserting the iddq pin. This will bring to life the input clock buffers in the common block. Simple measurement of the band gap voltage via the analogue test bus should confirm the correct 1.2 volt reference is present.

3.4 Power supply noise

Initial measurements of the inherent quiescent state power supply noise will be taken to ascertain the systems noise (i.e. the card and NOT the chip's). After the relative value is known for the inherent power supply noise the same measurements can be repeated with the chip fitted and fully enabled. The fully enabled state for the chip in this case includes the MoSys ram being fully powered up/operational, in this mode we should be able to observe any increase in power supply noise.

3.5 High Speed Clock Quality

Testing of the high speed clock quality is challenging but not impossible. The quality of the board level clock should be known from the commissioning stage of the test card. It is therefore feasible to assume that if the reference clock is clean entering the chip that the quality is sufficient internally for the PLL to lock to it. In addition to being able to measure the reference clock we have the ability to measure the reference clock after it has been buffered in the analogue domain, converted to a single ended version of the analogue clock and passed back out of the digital core via the clock tree. Measurement of the usual criteria, amplitude, rise/fall times, duty-cycle, and jitter will provide a reasonable indicator of the low speed clock path internal to the device.

To further ascertain the quality of the high speed clock requires the transmission of a continual one, zero pattern. Transmission of such a pattern will illustrate the in-phase clocks relative quality due to the final interleave multiplexer being clocked using this in-phase clock. Providing the resultant data-stream is observed to be "clean" we can infer from this that the high speed clock is of a good quality. Measurements can be made on the relative data stream for jitter, amplitude, and rise/fall times. An increase in jitter should be expected from the measurements as a result of the internal deterministic and random source of jitter in addition to the reference jitter.

3.6 Status Flags

There are a number of status signals passed from the transceiver to the digital core during initialisation, and setup of the link. These can be easily observed via the backend access ports from the core to the FPGA. Putting the transceiver into its various states and viewing the results of the status signals on the logic analyser will indicate correct operation of the status signals.

3.7 PLL Lock and Acquisition

The method for confirming PLL lock is via the output of the built in PLL lock detect circuit. Simply applying the reference clock applying the correct enables to the common block will allow the PLL to lock to the incoming reference. Monitoring of the lock detect signal on a scope will confirm to within a few Megs that the PLL is phase/frequency locked. Using the storage ability of the low speed scope in conjunction with a reference clock being applied should allow a measurement of the lock/acquisition time.

To further test the PLL for locking/tracking range the reference frequency can be moved up and down to determine the maxima and minima for the PLL input reference.

3.8 Mode Control

Testing of the mode control is a two fold exercise. Firstly the various modes of POR, reset, and enable need to be exercised for verification of their operation. Once the operation of the various control signals has been established the transceiver can be put into its various operating modes, i.e. Terachannel or PCI. This can be cross checked with the prior simulations to validate correct operation/signal polarity.

3.9 TX Transmission Testing

The first sets of tests that can be applied to the transceiver which will give an indication of relative operation are the drive and polling tests of the Tx cell. The Tx cell consists of three parts, each one being dependent on correct operation of the previous part in order to function correctly. Looking from the core side in the Tx consists of a cmos logic block, a high speed serialiser, and a high speed driver amplifier. All of these block level components can be enabled and rest individually. For successful transmission of any information the cmos block has to first correctly collect the data and control information from the core logic. Secondly the duty-cycle correction circuit, load generator and serialiser have to all operate and correctly clock the data through. Finally the high speed driver has to be powered up and be connected to a 50 ohm load. Assuming all this has happened and worked correctly data patterns should be observed on the Tx package pins.

The requirement to measure duty cycle error and high speed clock quality can be carried out in conjunction as in both cases the transmitter must be working and transmitting a continual pattern of one, zero. Using the high speed scope a simple persistence plot of the data stream measured against the inbuilt duty cycle measure function will give a good view as to the output duty cycle. The quality of the duty cycle in this case shows that the high speed clocks mark space ratio and that the output mux/high speed driver cells are well matched with minimum offsets.

A further measurement of transmission jitter on the output edge transition should be taken via the in built jitter histogram function of the scope. This will give a qualitative measure of both the high speed clock jitter plus the addition of subsequent jitter due to the Tx cells and associated interconnect in the package.

3.10 Link Alignment

The alignment of the link is one of the most critical stages of the testing as failure to perform correct alignment will negate any further Tx to Rx testing. In simple terms the application of a data stream to the Rx inputs should force the link to achieve bit alignment due to the nature of the phase interpolator/recovery filter operation. The actual alignment of the link is however more complex as bit alignment is only half of the problem.

3.11 RX Receiver Testing

To test the receiver in the first instance a full cml level signal will be applied to the Rx pins using a ten ones ten zeros pattern. This is to be subsequently followed by a continual one, zero pattern and finally a series of odd/even K28.5 characters. Driving the Rx in this manner removes any uncertainties due to the interconnect or physical environment. The inclusion of the above test patterns has the specific effect of testing both the Tx interconnect and the Rx portions for both low, high and broad band frequency spectrums. If the Rx is to have and difficulties in the range of frequencies it can cope with the described test patterns should uncover any adverse behaviours.

Using any of the predetermined patterns above will allow a very quick indication as to weather the Rx has managed to a) receive any signal through its input amplifier and b) determine if the bit sync detection mechanism has managed to lock on to the bit boundary of the high speed serial stream. Simple observation of the bit byte sync flag with the sync enable set to the appropriate mode will confirm if the PI has locked onto the incoming bit boundaries successfully.

Further testing of the synchronisation mechanism will be carried out by using the preset sync character in duel polarity mode and moving the sync enable from bit to byte sync. As with bit synchronisation simple observation of the sync flag will determine if the pre-programmed byte character has been captured and correctly aligned to in the capture register.

3.12 Duty Cycle Testing

Testing of duty cycle accuracy in relation to the Tx portion of the device is none complicated, a simple toggling stream of '1' '0' patterns fed into the serialiser will produce a high low data stream that changes on the bit position. Measuring the bit stream with the high bandwidth scopes built in functions will produce an accurate measurement of the transmit duty cycle.

Testing of the Rx is somewhat more complex involving manual movement of the phase Interpolator. As in the case of the Tx cell a continual '1' '0' pattern needs to be produced and fed into the receivers inputs, once the Rx is locked onto the bit boundary the interpolator can be used to measure the various bit widths. Stepping the Interpolator across the bits inside the de-serialiser whilst observing the output parallel field on the logic analyser, should allow a count to be realised for each of the bits. Each of the bits should measure approximately 60+ phase steps, having a measurement for all 10 bits in the de-serialiser allows us to make an approximation of the Rx duty cycle.

3.13 Synchronisation Character Tests

Built into the transceiver is the ability to reprogram the Sync register to lock to a different character, by default it looks for K28.5. In order to test the Sync registers ability to lock to other characters the register simply has to be set to use an alternative byte pattern. Observation of the bit-byte-sync flag will confirm if the sync register is correctly locking onto the byte boundary with any reprogrammed synchronisation character.

3.14 Transmission Jitter (Phase Noise)

Measurement of the transmission Jitter will be carried out during the testing of the Tx unit, connecting the Tx output to the scope and using the inbuilt Jitter histogram functions allows for an accurate measurement of the Jitter profile. If it is felt necessary to make a more detailed set of measurements then use of other test equipment i.e. a spectrum analyser will be necessary.

3.15 Amplitude Level Adjustment

The transceiver has designed into it the ability to alter its drive strength and hence its output amplitude. It is necessary therefore to measure the level of adjustment obtainable with the built in flexibility. This series of tests can again be carried out as part of the Tx unit investigations.

3.16 Pre-emphasis Settings

Owing to the fact that the transceiver operates at such a high data rate (high frequency) the output Tx cell has been designed with the ability to pre-distort the output signal. Having the ability to alter the output signal in this manner gives the transceiver compensation ability to cope with frequency dependent losses associated with majority of transmission media. Testing of this portion of the Tx cell is critical to device being suitable for TeraChannel applications. As with the amplitude tests the pre-emphasis tests will be carried out during the Tx unit testing. Observation of the signal into the high speed scope will illustrate the transmitters emphasis capabilities, the Tx has enough built in compensation to drive an additional 4.8dBs of over emphasis onto a signal edge.

3.17 BER Testing

BER testing is in reality the acid test; this provides quantitative measurements of the devices signal to noise performance. BER testing will be carried out as a series of soak tests across different interconnects and across individual devices as well as different devices connected together. For the BER testing to be possible majority of the major portions of the whole transceiver must be functional correct and working within specification. BER setup involves the alignment of the Rx to the Tx end (both bit and Byte) with the switching in of the PRBS sequence only when alignment is fully achieved. The transceiver has been designed to have a target BER of 1e-12 or better, to further test the flexibility/range of the transceiver different lengths of cable and interconnect (physical media) will be used.

4 TEST RESULTS

The following section captures the results and outcome of the testing exercise carried out during the testchip debug. Testing should follow the test strategy described in section 4, it should be made clear however that the test strategy outline may not necessarily be adhered to rigorously.

4.1 Power, clock and reset tests

The FPGA had a simplistic set of instructions coded into it which allowed the chip to be powered up and simple connections to be made to the testchip. The chip was put into Iddq mode to check the static current consumption, and successfully brought back out of Iddq mode. The indications from this simple series of tests were that the chip was live and free of any initial problems.

The testchip was been further tested via application of a 250MHz PECL clock on its reference inputs. The PECL clock was successfully converted into a single ended cmos version inside the common block, passed through the core clock tree and buffered back in and out of the FPGA.

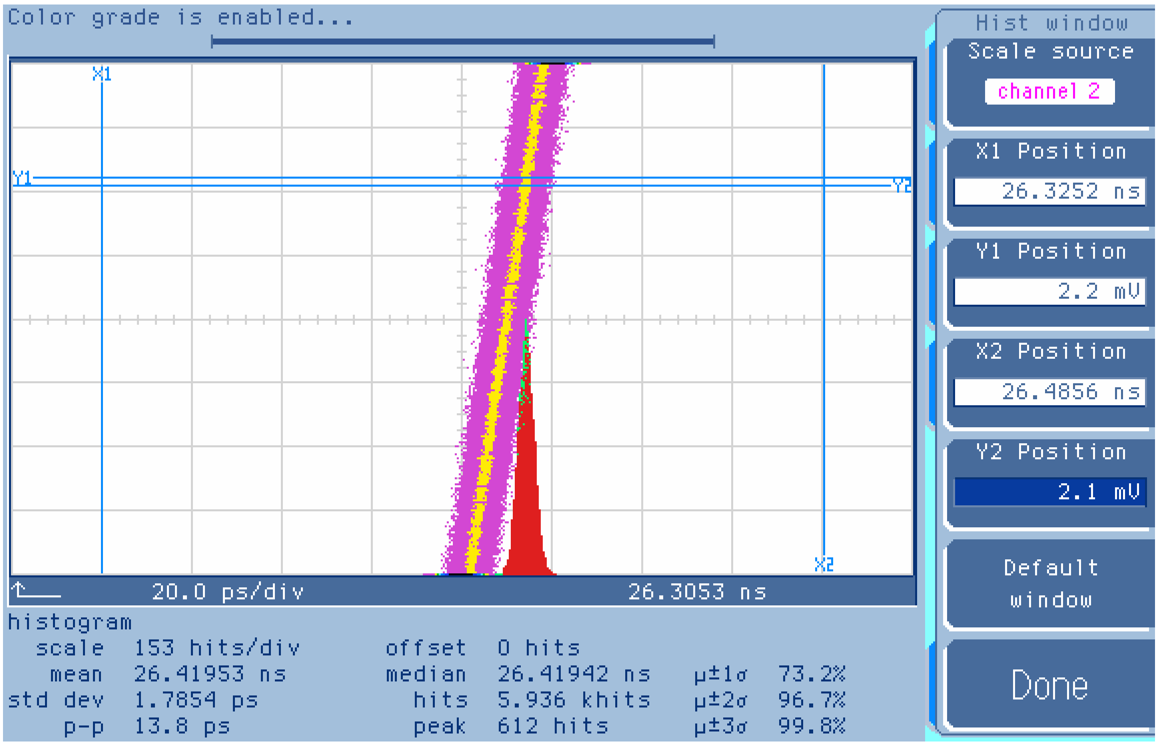
The code for the FPGA has been implemented in such a way as to allow the common block to be taken from the power down mode to reset and finally into running mode.

4.2 Status flag tests

Further testing of the common block has proven completely successful, using a predefined set of connections on the common block core inputs, It was verifyed that the high speed PLL’s lock detect circuit is indicating lock when the PLL_en is driven into it’s active state. This further provides proof of both PLL functionality and correct operation. We have also been able to repeatedly observe the lock detect being activated and de-activated as the PLL_en line is driven high and low. We are therefore now able to successfully take the device common block through the modes described above.

4.3 TX operation and power dissipation tests

Other investigations were in relation to the high speed measurement environment, the high speed scope and the 2.5GHz probes have been successfully connected and function. The reference jitter has been measured with the scope (to a first order) in the region of 2ps RMS or approximately 16ps pk-pk. See the scope Plot 1 below:



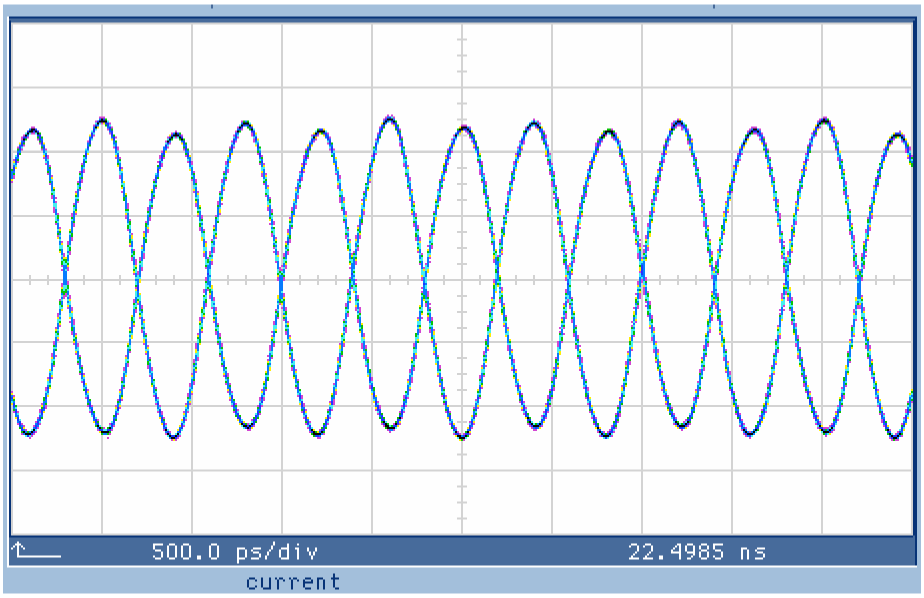
Plot 1

As discussed previously the efforts have been concentrated on the Tx cell of transceiver 0. The Tx device was exercised in a similar manner to the Common block with a series of modes being defined and coded into the FPGA..

The Tx block was initially put into a power down state, at this point the 'off' mode current is within a sensible range as. there is no noticeable change on the power supplies current indicator.

4.4 TX signal quality tests

The Tx block was then passed through reset into running mode 1, whereby the FPGA codes a continual stream of alternating '1,0' bits onto the Tx parallel data inputs. This was clearly observed on the Tx output serial pins with a clean waveform being output. Plot 2.



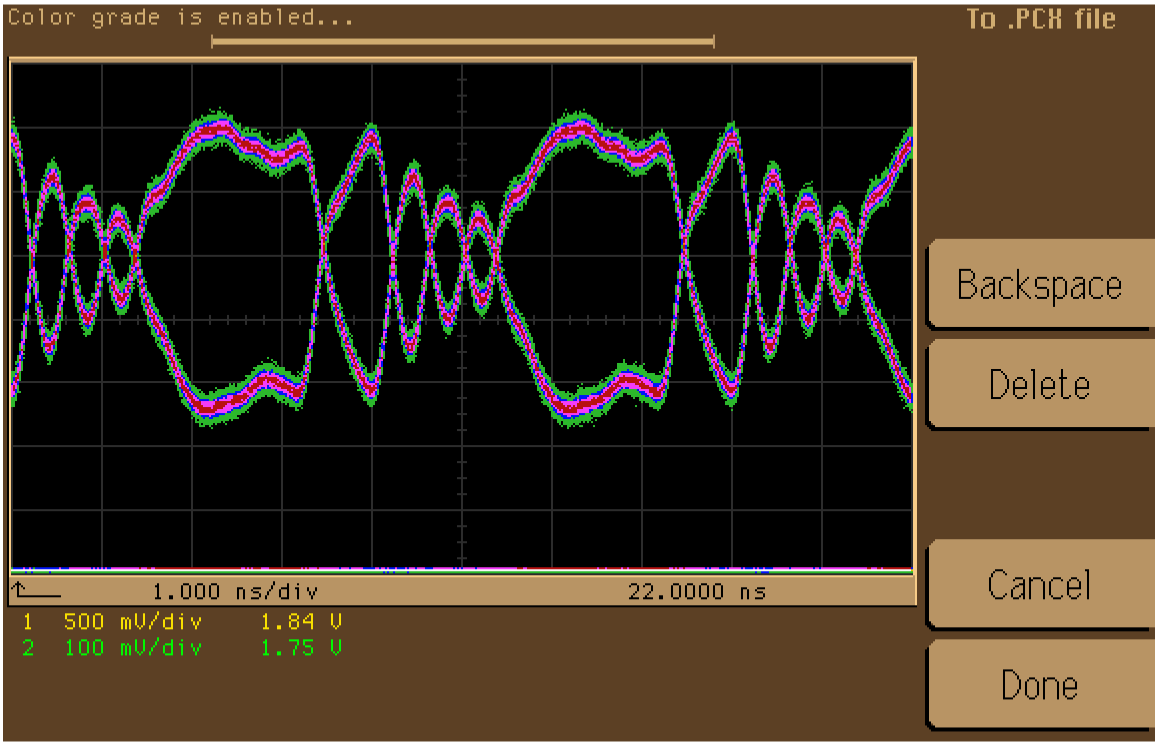
Plot 2

Driving the device in this way validates that the various levels of multiplexing within the core are operational and functioning as designed, also that the Tx elastic buffer is operating in the correct manner with no clock boundary problems. Plot 2 shows illustrates the high quality of the Tx signal, indicating correct opperation of the Driver cell load generator, duty-cycle correction circuit and serialiser are all functioning, effectively verifying the entire Tx cell.

Measurements of the data eye in this mode revealed a transmission duty-cycle of 49/51. Measurement of the transmission jitter for even data gives a 50ps Pk-Pk Jitter which exceeds the requirements for both TerraChannel devices and PCI-Ex.

The FPGA was modified to generate K28.5 odd and even continually, this being a much more stringent test of the Tx cells transmission capabilities as K28.5 data generates a significantly wider band of frequencies.

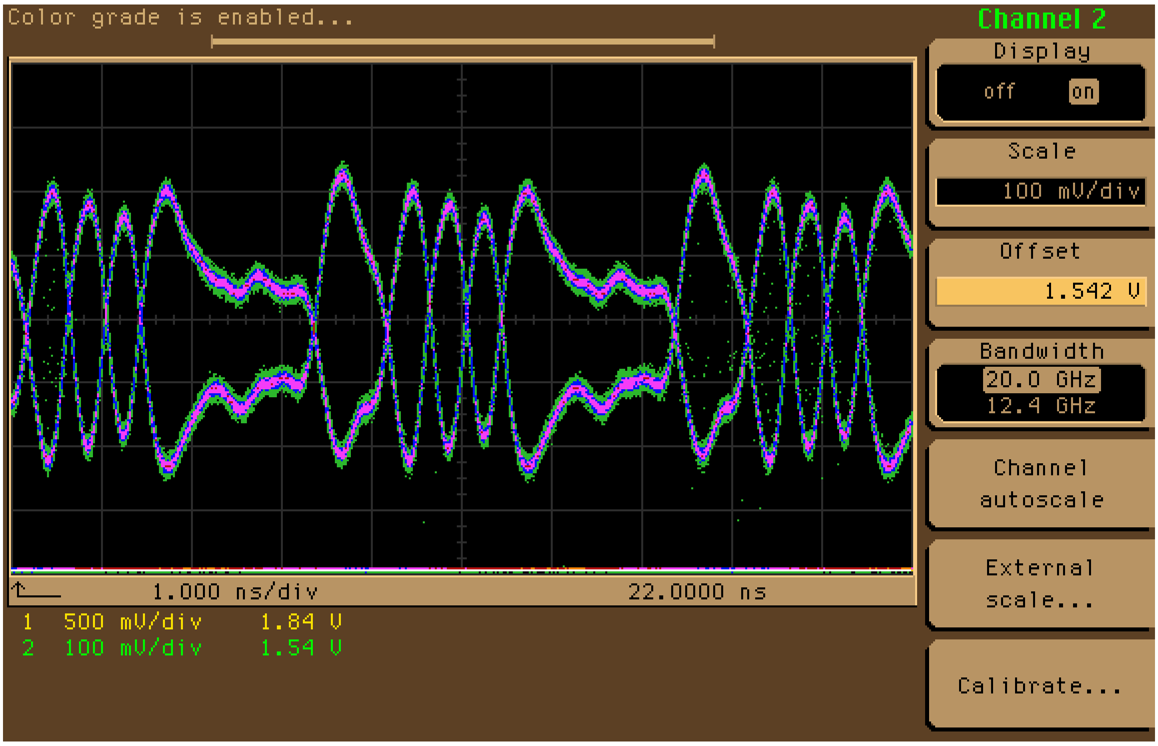
Testing of the Tx in this mode revealed clear eye patterns observed at the test load. Plot 3 below shows the scope output: note that most of the ISI/BW limit is due to a direct result of the probe BW limits.



Plot 3

The initial plot was with the driver amplitude programmed to minimal setting of 14mA output drive and no pre-emphasis.

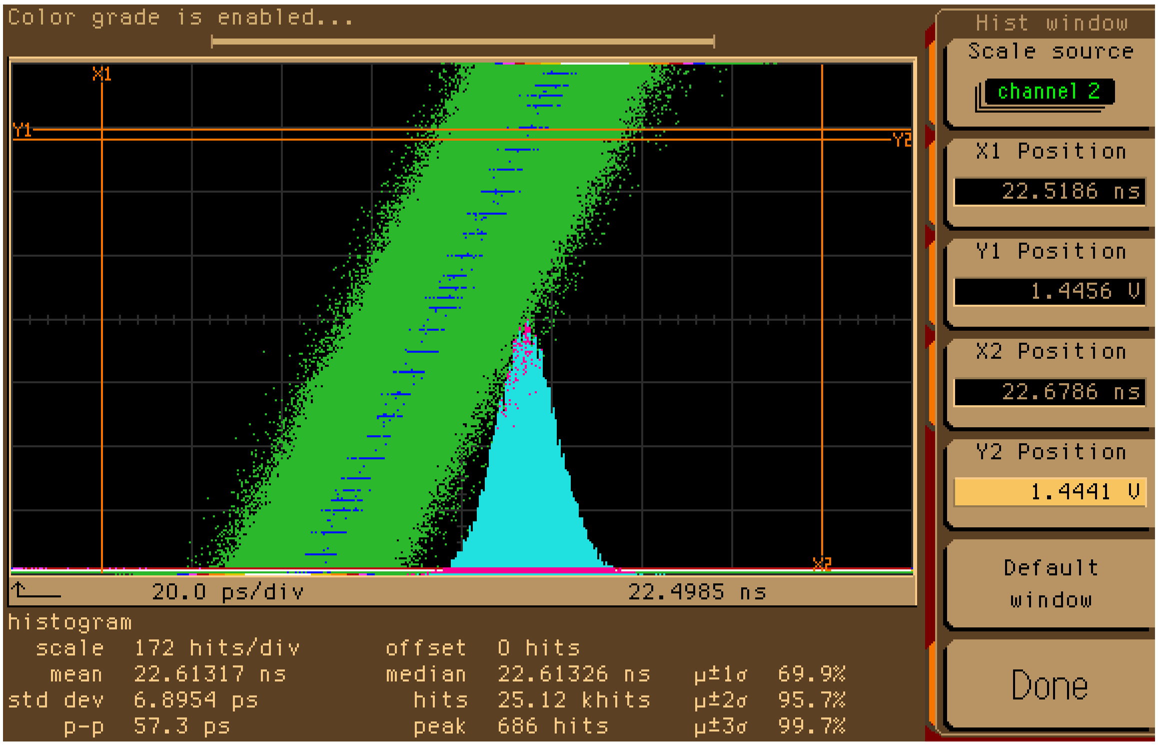
Further testing of the Tx K28.5 mode was undertaken with the driver's amplitude being left at minimum but with the full 4.8dB of emphasis being turned on, the result was as designed with low frequencies clearly being compressed and the high frequencies being amplified. This can be viewed below, Plot 4



Plot 4

The Tx cell has been exercised through its whole range of amplitude settings and its whole range of pre-emphasis settings with the results observed that the test load behaved as designed.

The final series of data measured the Tx transmission jitter on the K28.5 character. The result being 57.3ps Pk-Pk or 6.8ps RMS which was well within the required limits for PCI-Ex. It should also be noted that the measurements and results taken for the transmission jitter include the internal scope jitter. A final scope plot of the Tx transmission jitter is viewable below, Plot 5



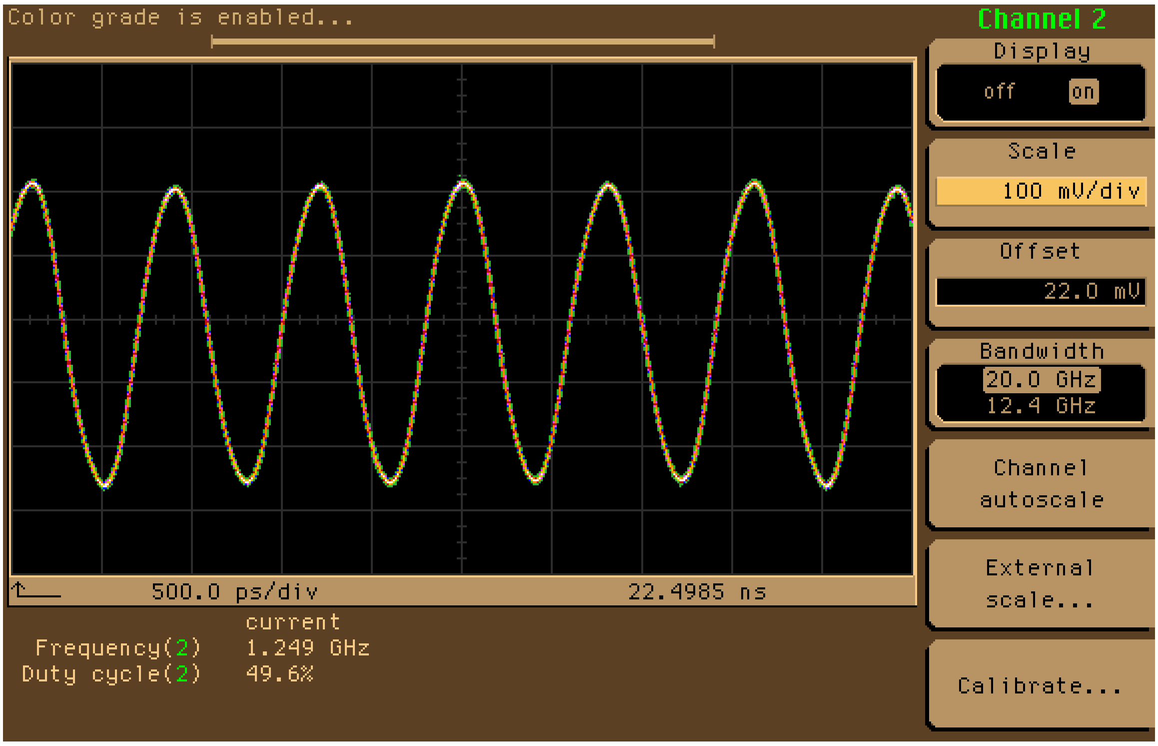
Plot 5

Final tests were to observe transmission and reception of K28.5 via internal loop back and then via the Gore cable assemblies.

The Tx cell has been fully exercised through all of its designed amplitude and pre-emphasis settings using a slightly different method of connecting to the scope.

Connecting to the scope via a 100nF AC coupling capacitor and a 50 ohm 70cm coaxial line allowed the full 20GHz bandwidth of the scope to be realised. Connecting in this manner uses the scope as the 50 termination for the Tx cell.

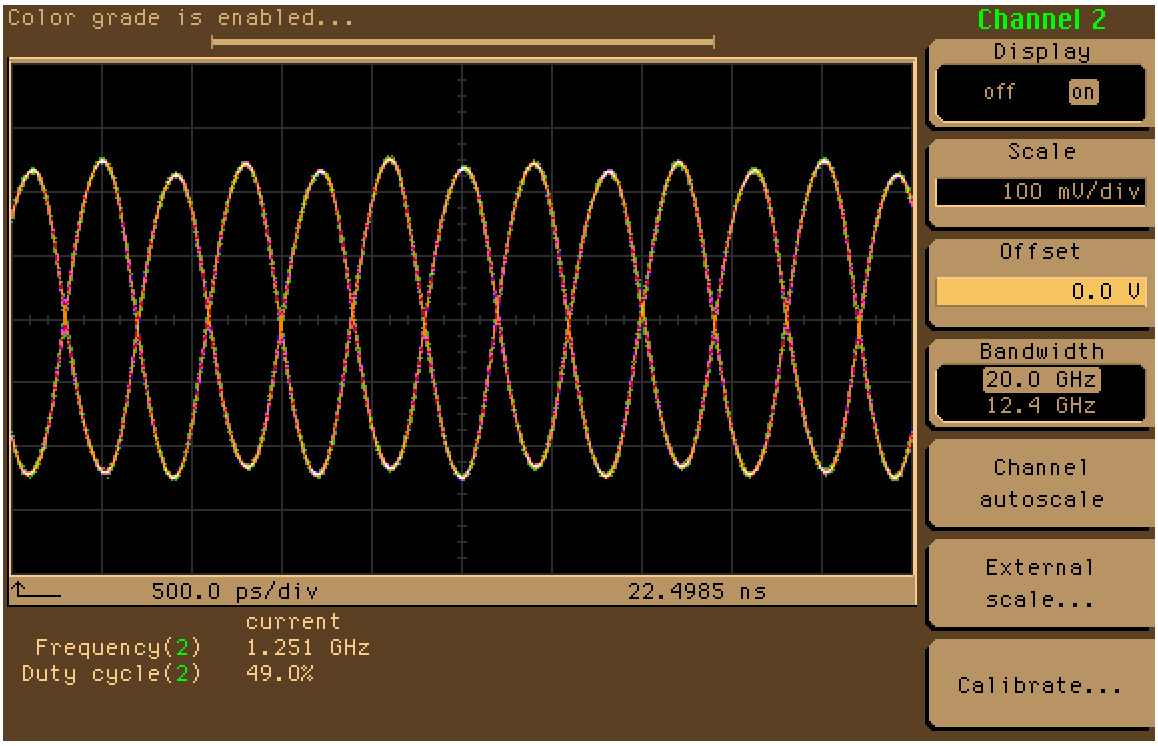
The plots obtained clearly show the ISI and Bandwidth limit that the 2.5GHz probes caused. Plot 6 below is of the 1010101010 pattern fed into the back of the transceiver.   .



Plot 6

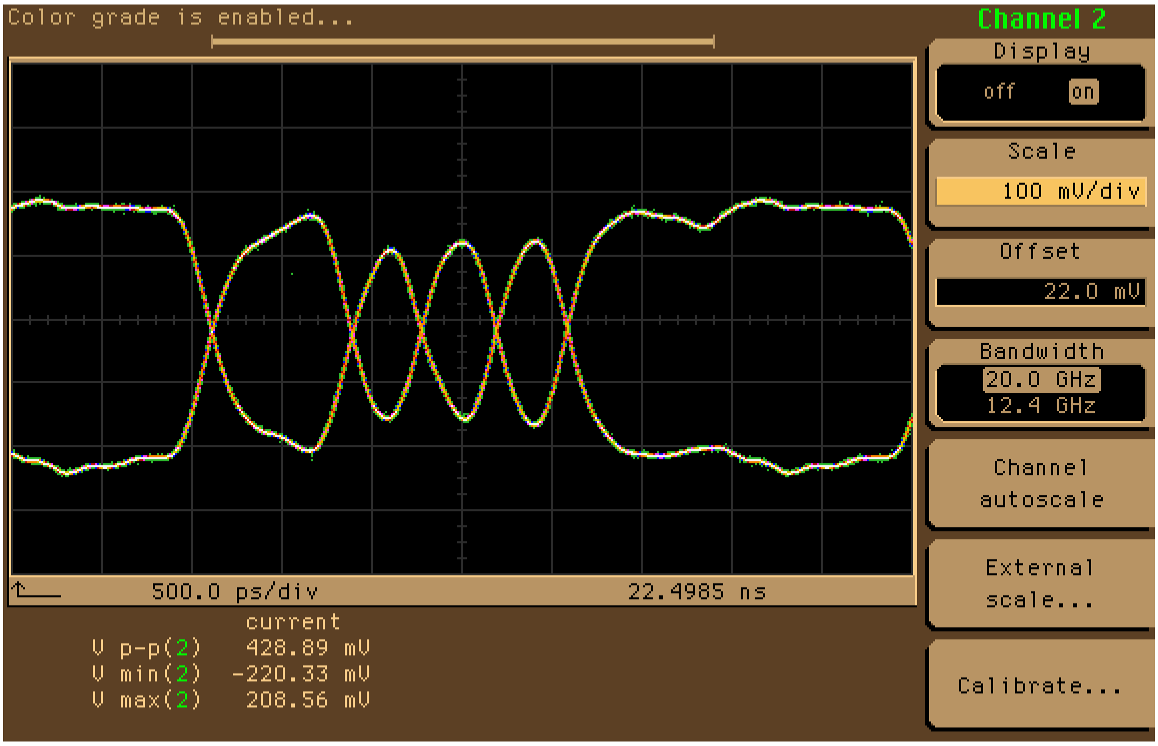
The duty-cycle is measured at better than 49/51 with transmission jitter measurement improving to 30ps Pk-Pk (still inclusive of scope jitter), the measured frequency of the constant pattern is 1.249 GHz.

Plot 7 is a full differential view of the previous 1010101010 pattern using the second channel of the scope in conjunction with the first. The amplitude distortion visible is largely due to component and scope channel mismatches between the two channels. Note the location of the centre crossings.



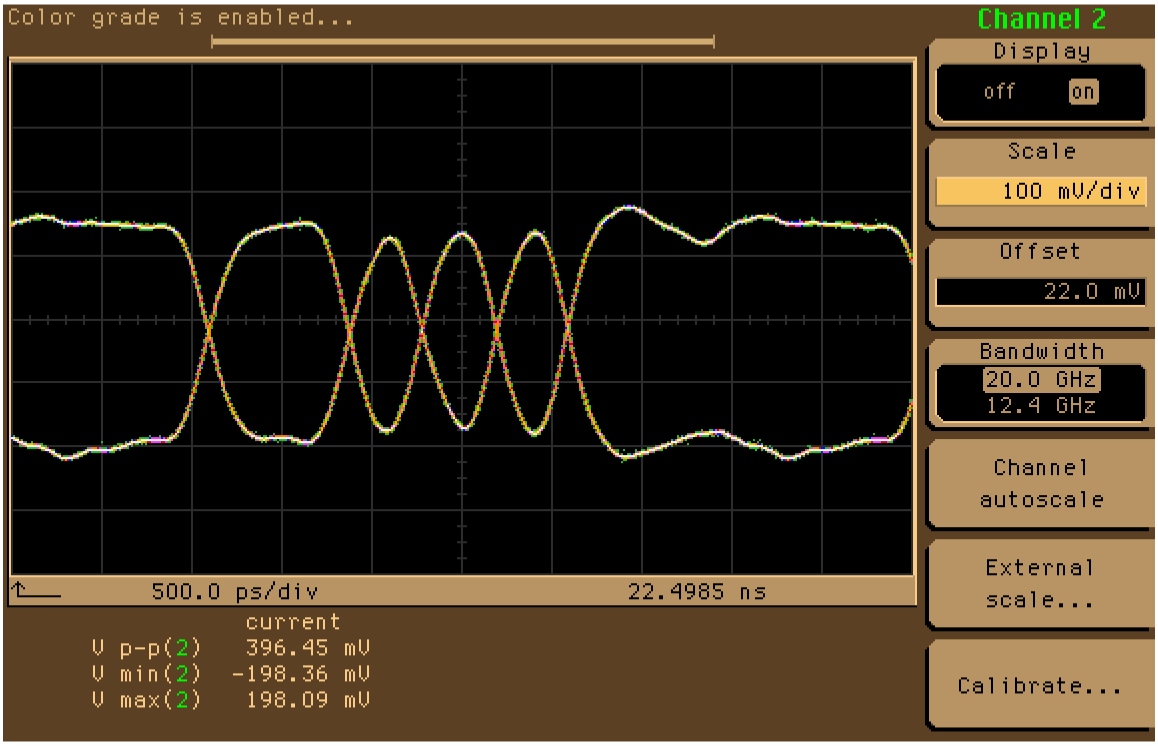
Plot 7

The next series of tests performed on the Tx cell involved exercising it through its full range of emphasis settings whilst applying minimum amplitude setting to the output driver. The test character used for this test was K28.5 which covers the widest spectrum of frequencies along with the worst case run length the Tx cell is likely to encounter.



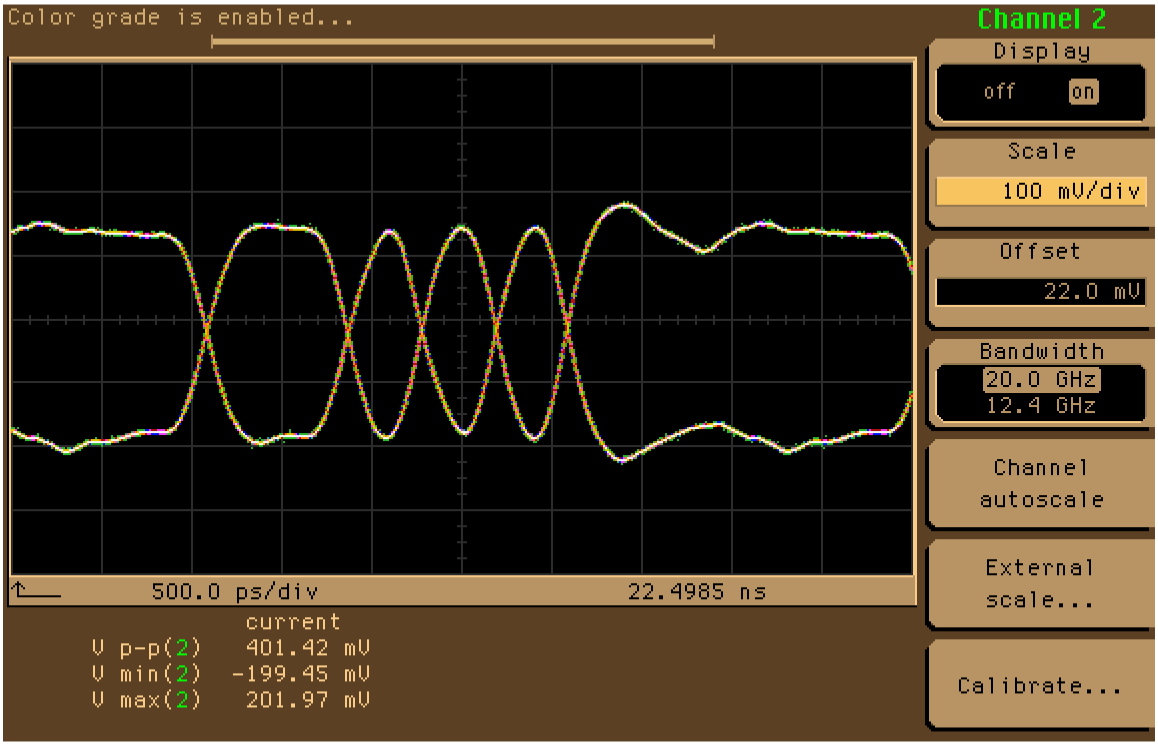
Plot 8

The observed output (Plot 8) is as expected with the DC (low frequency components) having a greater amplitude than the high frequency components. It should be noted that the clarity of the plot is exceptional when compared with the previous results using the 2.5GHz probes.



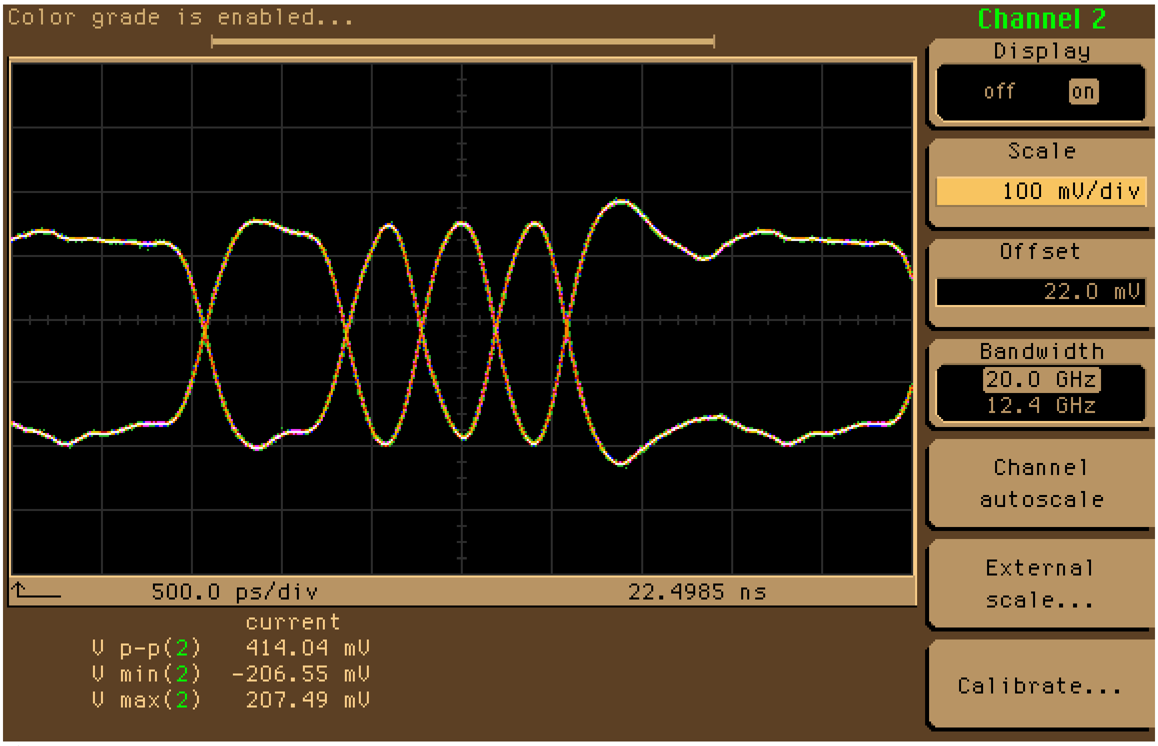
Plot 9

Plot 9 above is with a single bit's worth of pre-emphasis turned on adding approximately 1.4dBs of compensation. Even with such a small introduction of compensation the high frequency components are clearly improved when compared to the previous plot. (Plot 8)



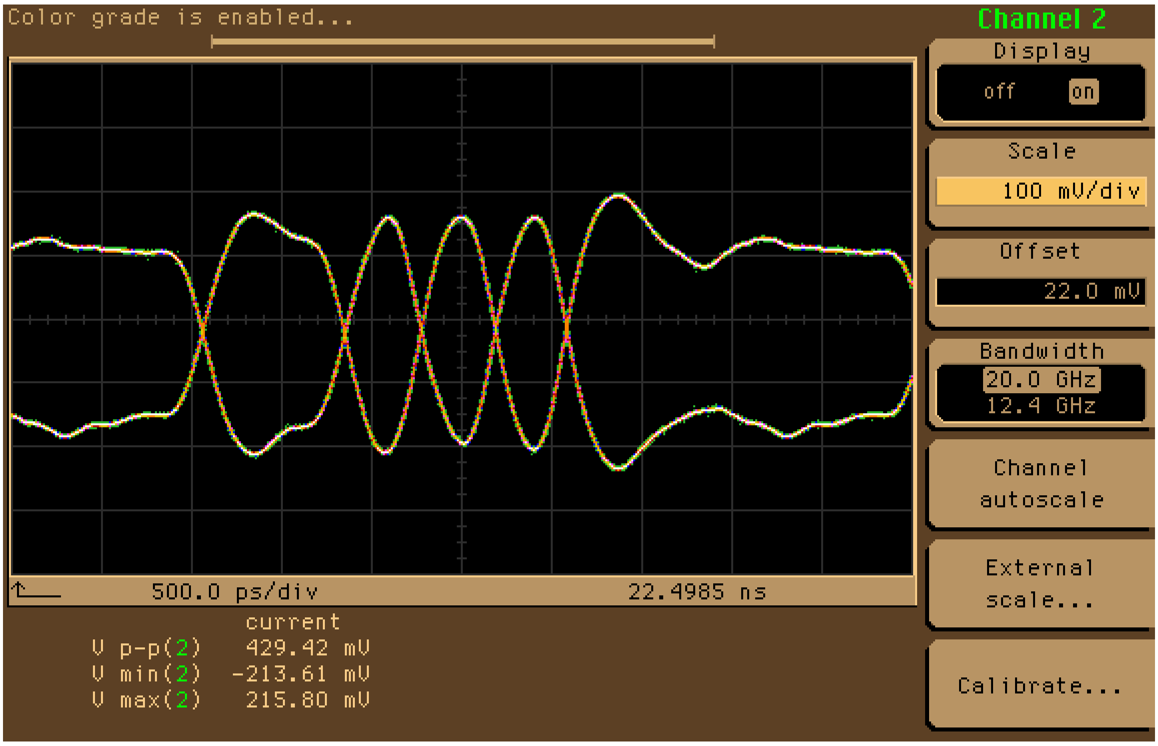
Plot 10

Plot 10 above has two bits worth of Pre-emphasis turned on (1.9dBs of compensation)



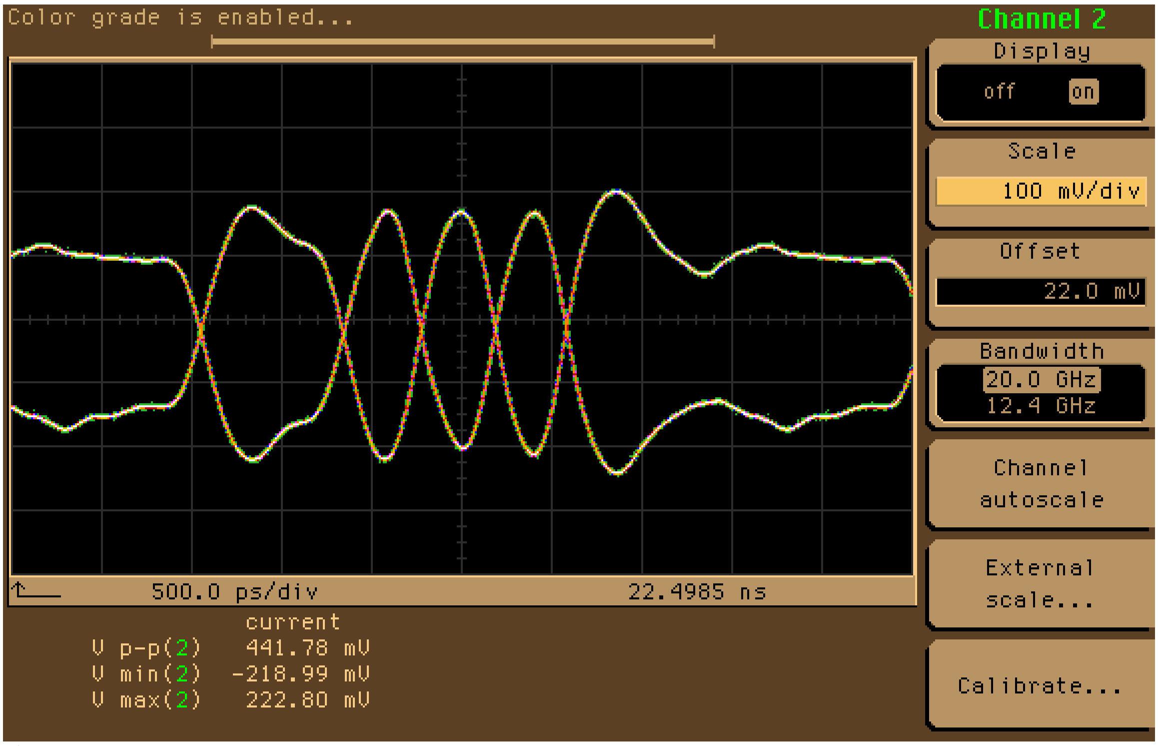
Plot 11

Plot 11 has 3 bits of Pre-emphasis turned on. (3dBs of compensation)



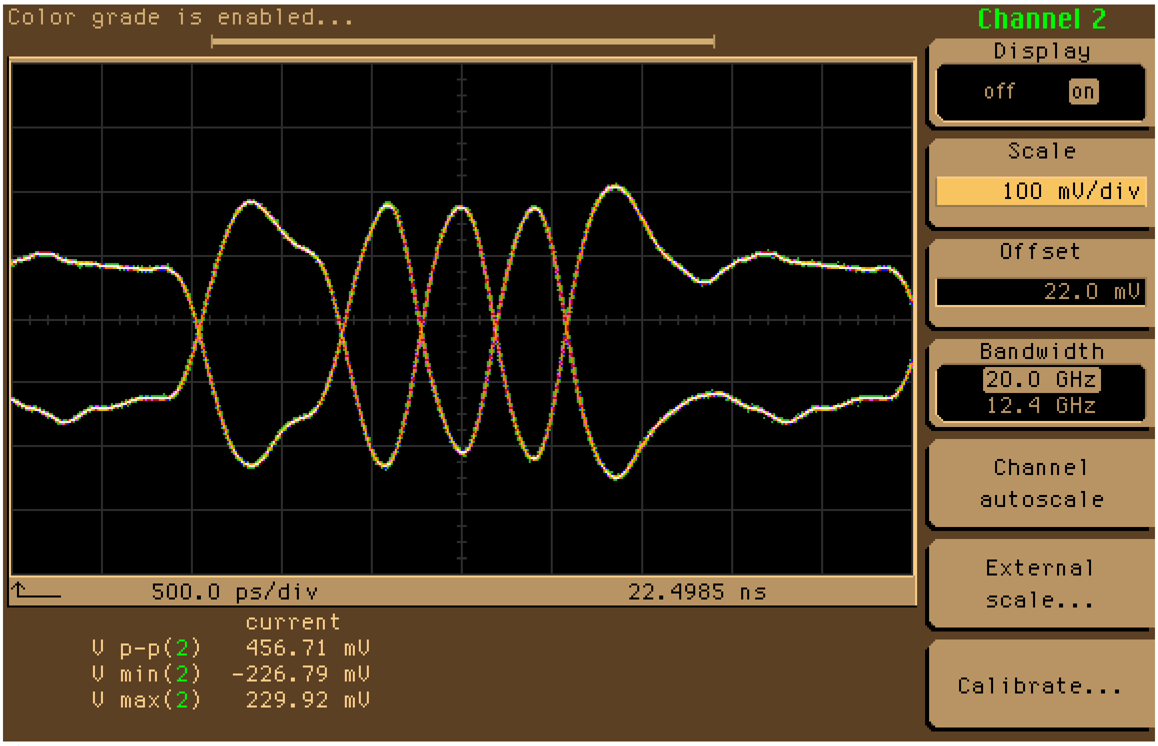
Plot 12

Plot 12 above has 4 bits worth of Pre-emphasis turned on. (2.5dBs of compensation)



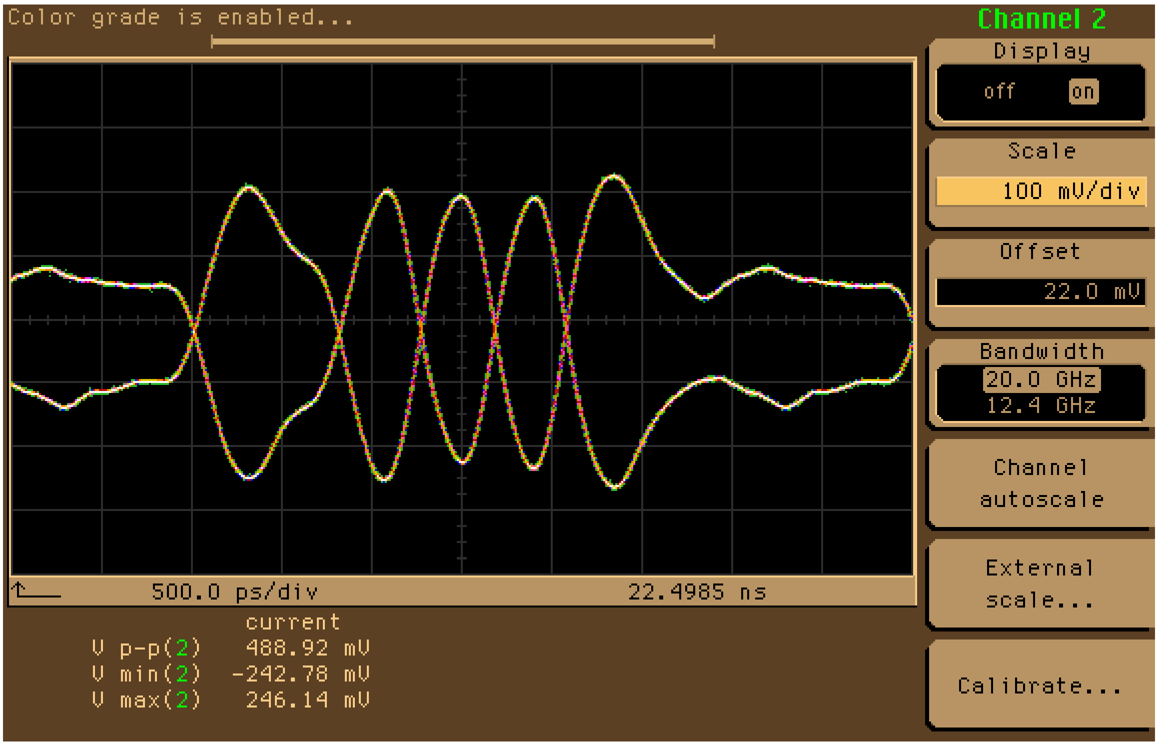
Plot 13

Plot 13 above has 5 bits worth of Pre-emphasis turned on. (3.5dBs of compensation)



Plot 14

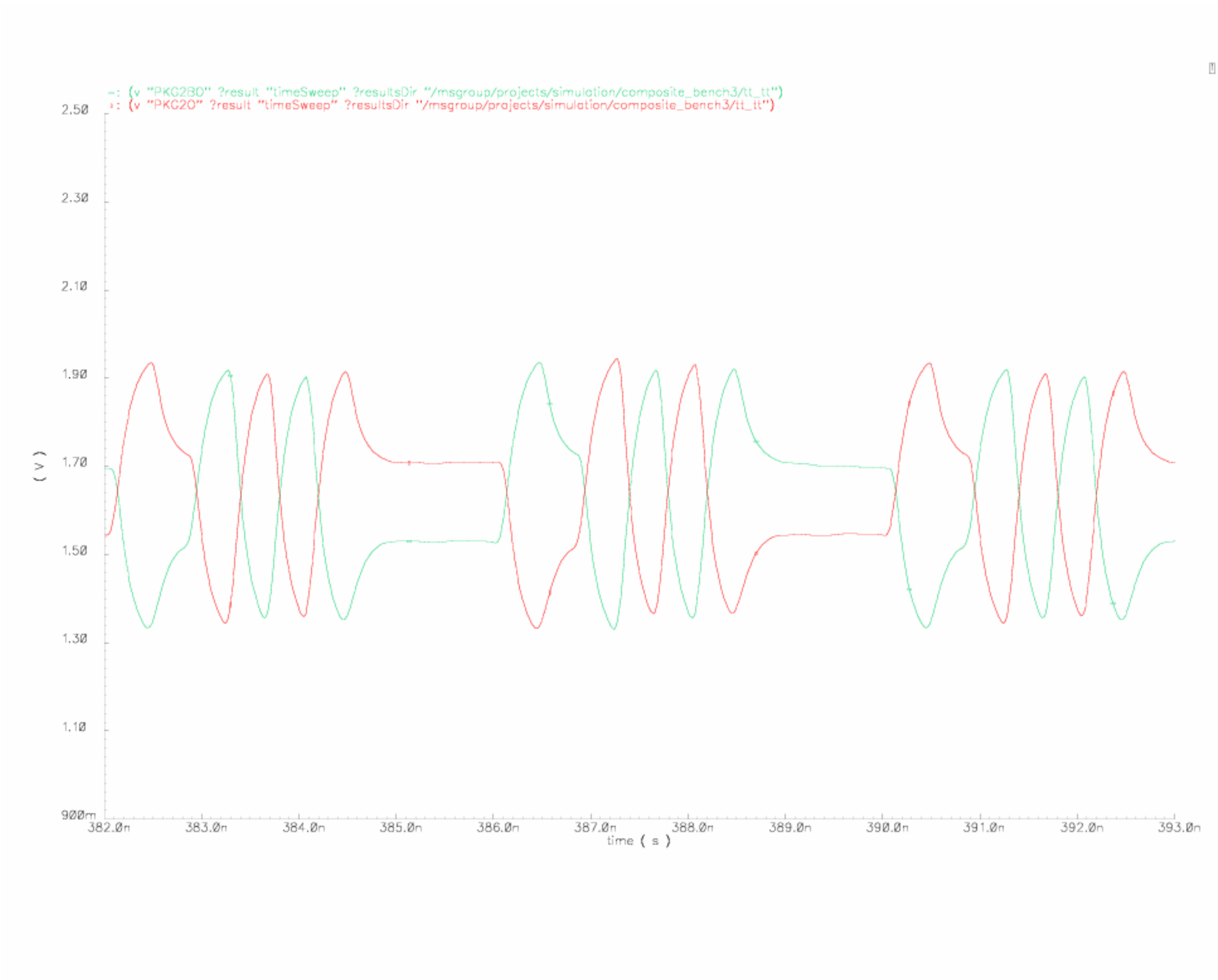
Plot 14 above has 6 bits worth of Pre-emphasis turned on (4dBs of compensation)



Plot 15

Finally the full amount of Pre-emphasis is switched in, clearly showing the effect on both the high and low frequency components.

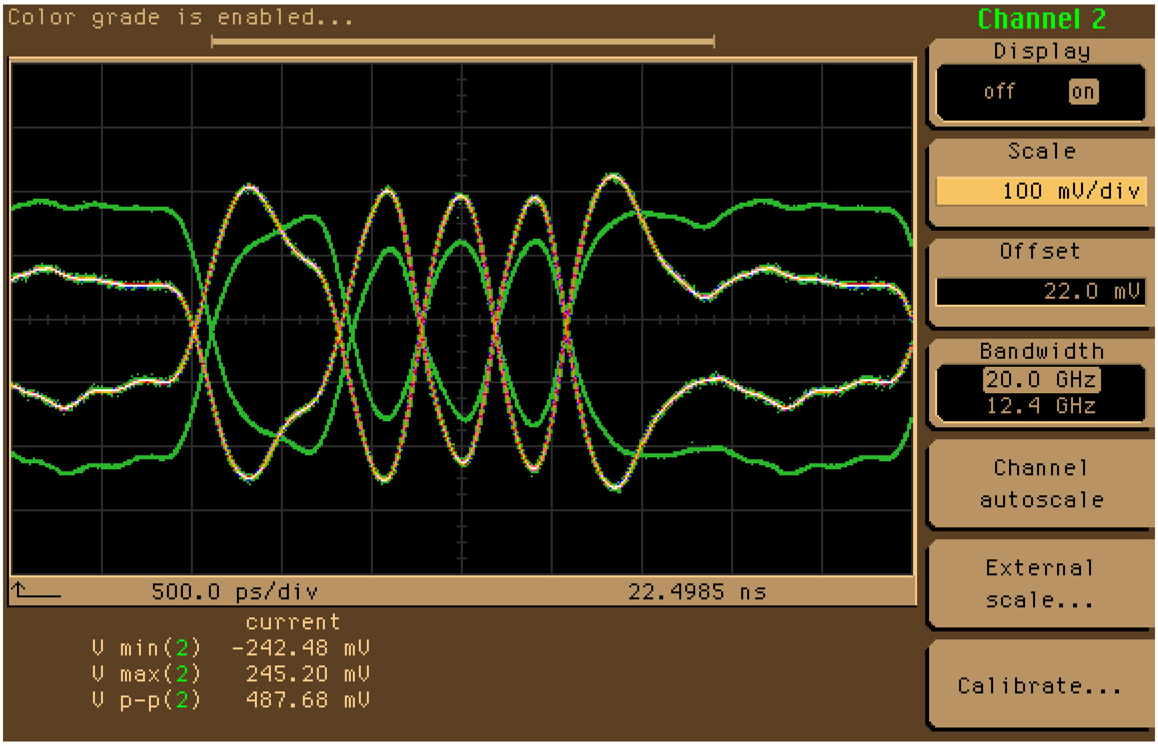
When comparing Plot 15 with the fully extracted version of the composite simulations, Plot 16 below, we can see the strong correlation between the silicon and the simulation results.



Plot 16

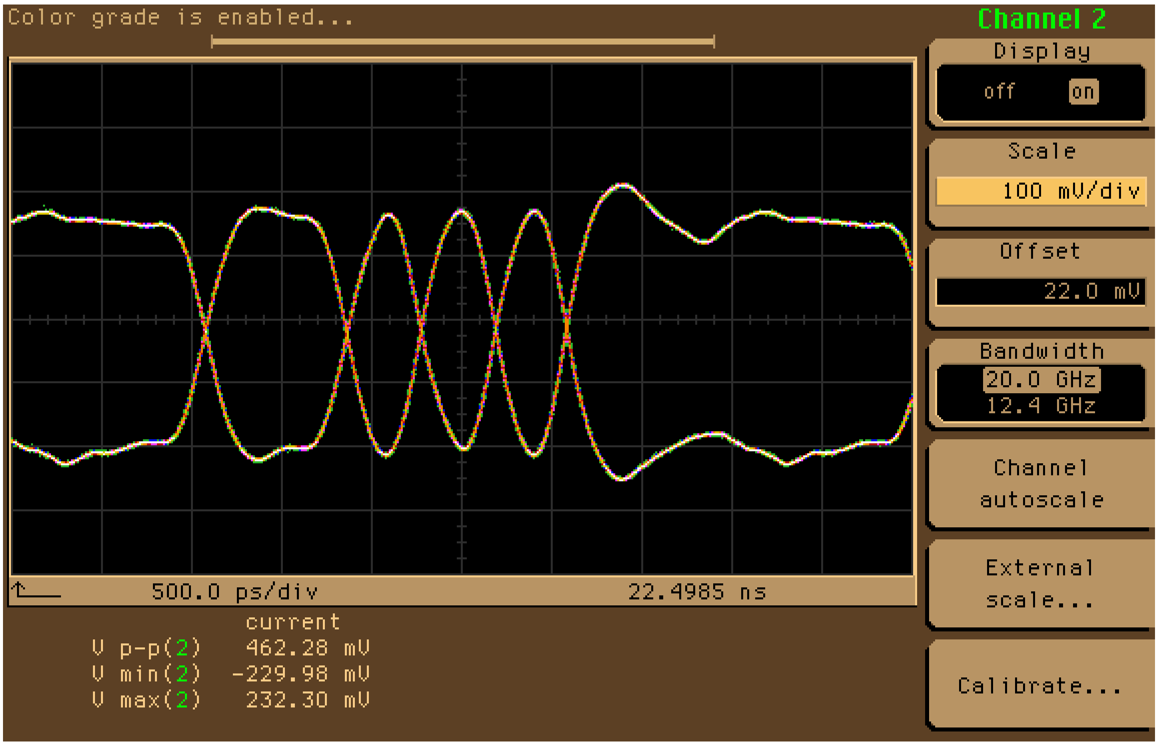
Plot 16 above plot shows the output from the composite simulations run on the Tx to Rx designs prior to tapeout of the device.

Finally Plot 17 below, shows the full effect of the Pre-emphasis shown with the white trace indicating the fully Pre-emphasised waveform and the green trace showing the original uncompensated waveform.



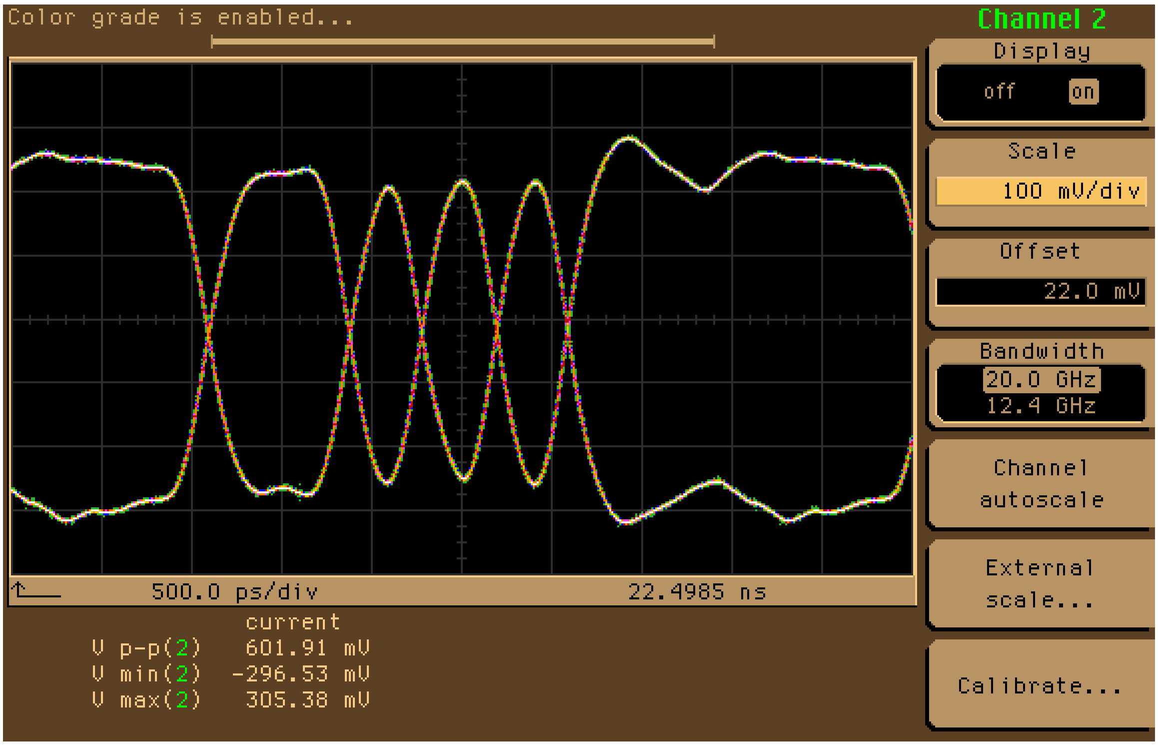
Plot 17

After exercising the full range of Pre-emphasis the amplitude drive was exercised for the TeraChannel modes. .



Plot 18

Plot 18 shows the transmitter driving out at 26mA

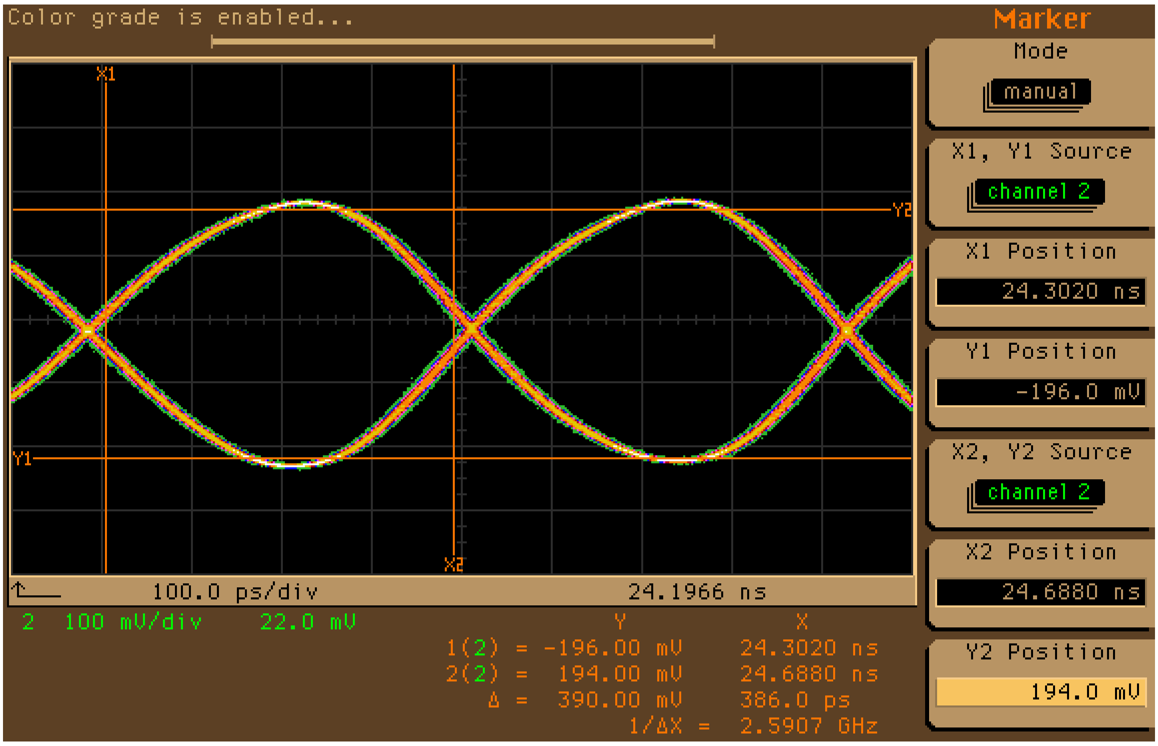


Plot 19

Plot 19 above has the transmitter driving out at the full 30mA

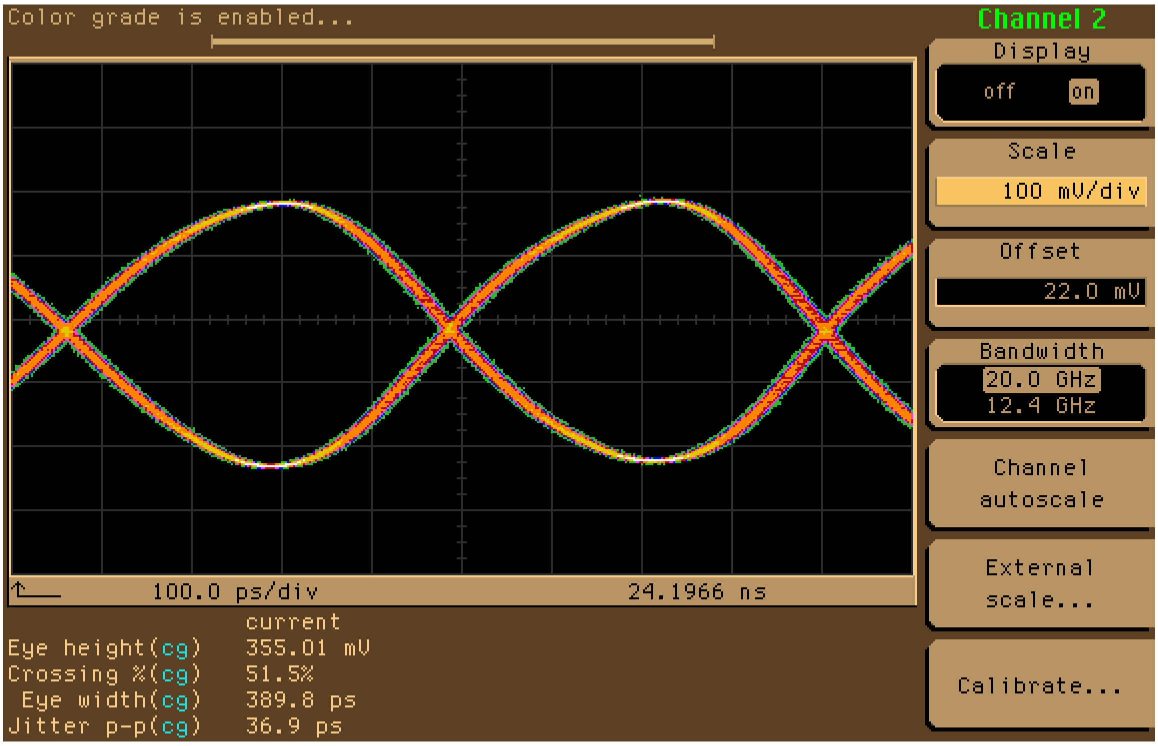
The final series of tests performed involved looking at the transmitter in the PCI modes designed in.

All the tests carried out were on channel zero with the scope again AC coupled with the 50 ohm coaxial cable. Measurements of the eye were taken both manually and via the scopes inbuilt eye function. The transmitted pattern used was again the K28.5 in toggle mode (odd/even).



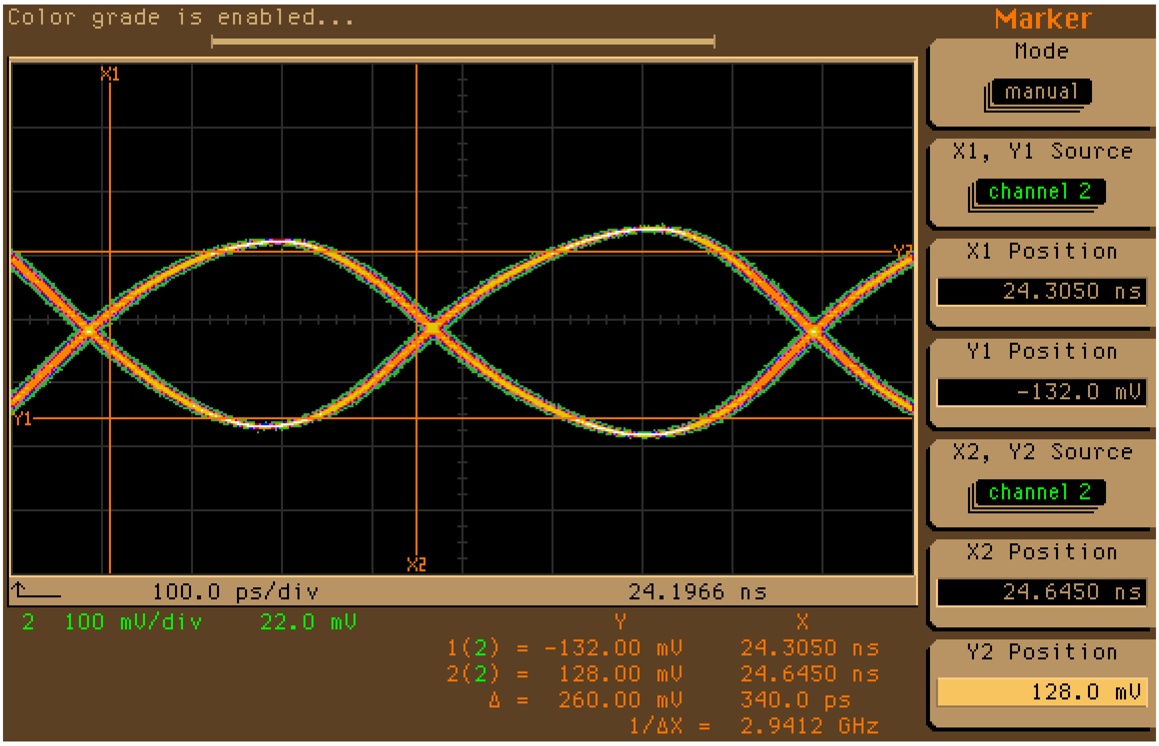
Plot 20

Plot 20 above is of the high frequency components of K28.5 using the manual markers to measure the data eye. The eye is very clearly open with relatively little transmission jitter. The settings for this particular measurement were 16mA of amplitude drive and 3.5dBs of Pre-emphasis.



Plot 21

Plot 21 above is as previous but using the scopes inbuilt eye measurement functions. The scope revealed a good measurement of the eye showing it to be well within spec for PCI compliancy. More importantly the transmission jitter measured at around 37ps Pk-Pk on the K character.

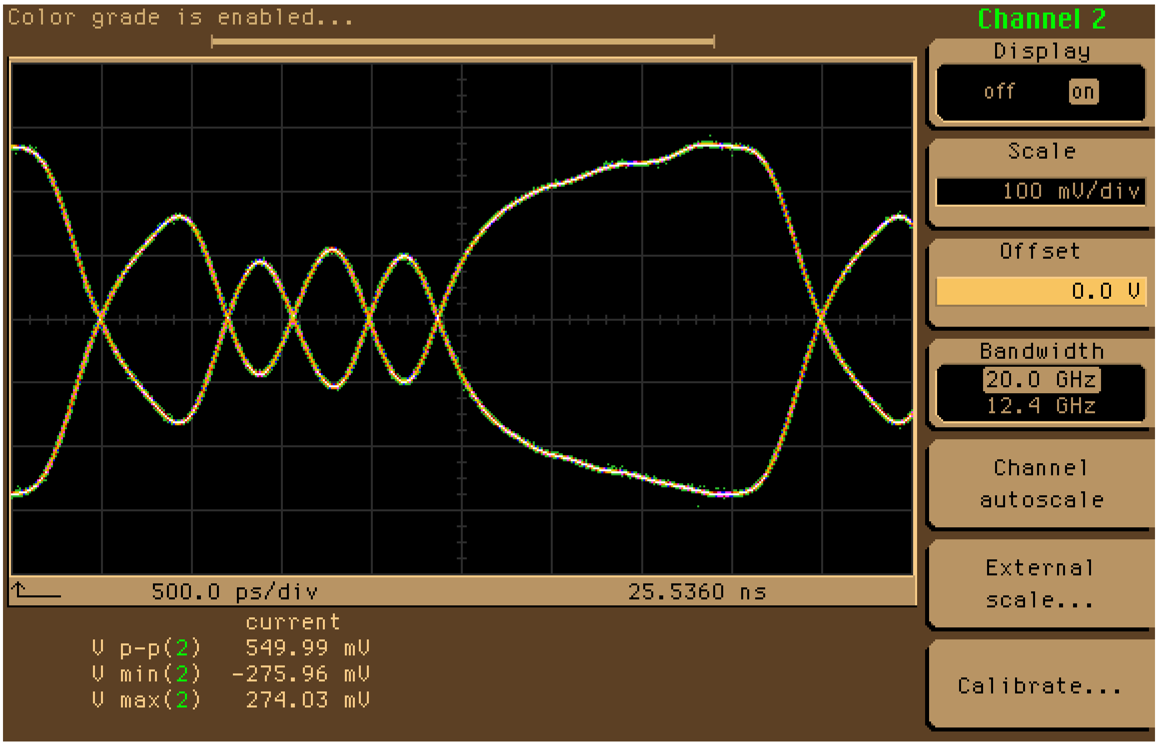


Plot 22

Plot 22 above shows the effect on the data eye when the Pre-emphasis is switched off. The amplitude can be seen to reduce and the eye can be seen to close up by some 46ps. Despite the degradation in the eye this should still be sufficient to resolve the bits in the receiver with satisfactory BER.

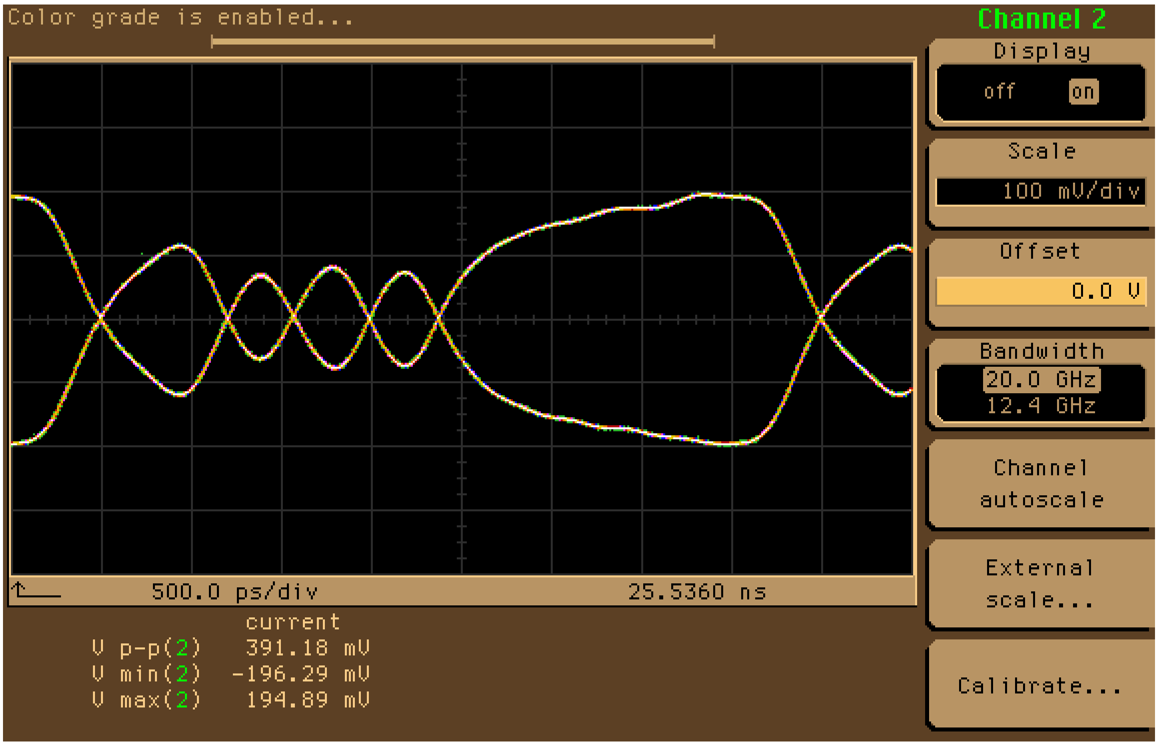
Testing with longer cables. The first series of tests were run with the chip AC coupled to the 20GHz scope using a 5M length of RG58U coaxial cable connected to the existing test rig. The Tx cell was capable of driving the 5M cable. Doubling the length of RG58U coaxial cable to 10M gave the result below.

The signal visible on the scope was of high clarity with exceptionally open eyes. Plots 23 - 27show the Tx cell driven into the scope via the existing 70cm of Coaxial cable into an RG223 SMA connector through the 10M of RG58U and finally terminated at the scope channel.



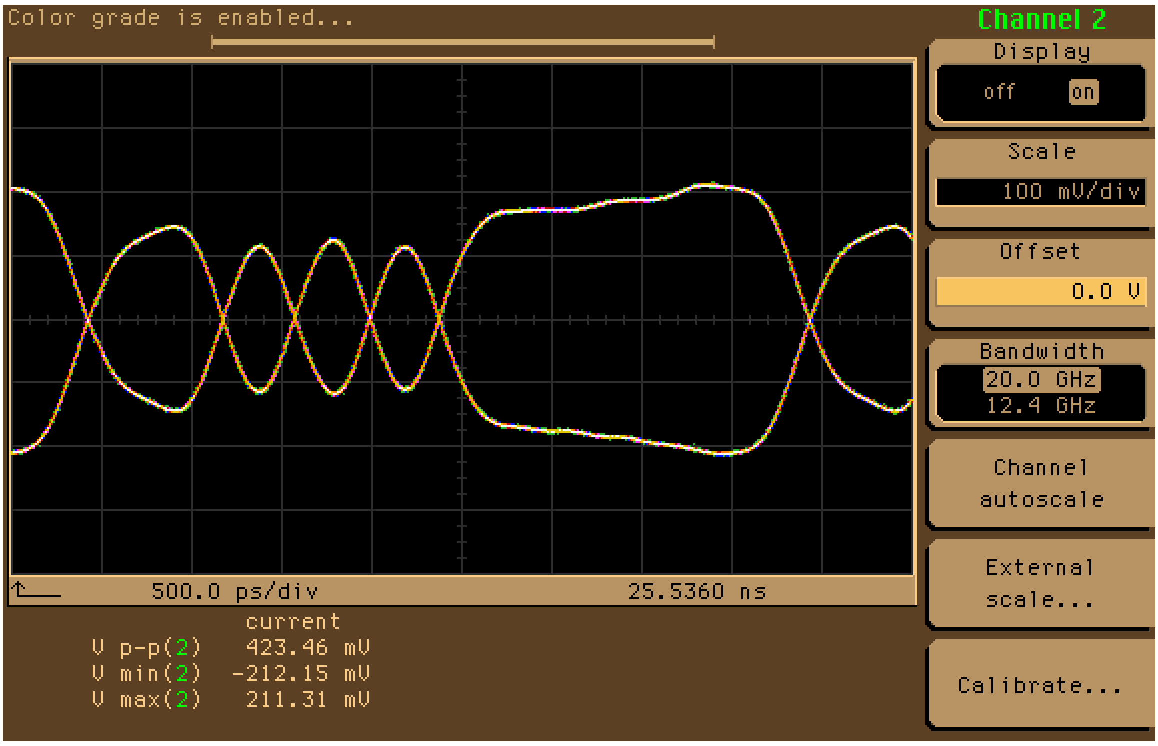
Plot 23

Plot 23 above is the result of driving the Tx cell through 10M of RG58U in PCI mode with no additional pre-emphasis.



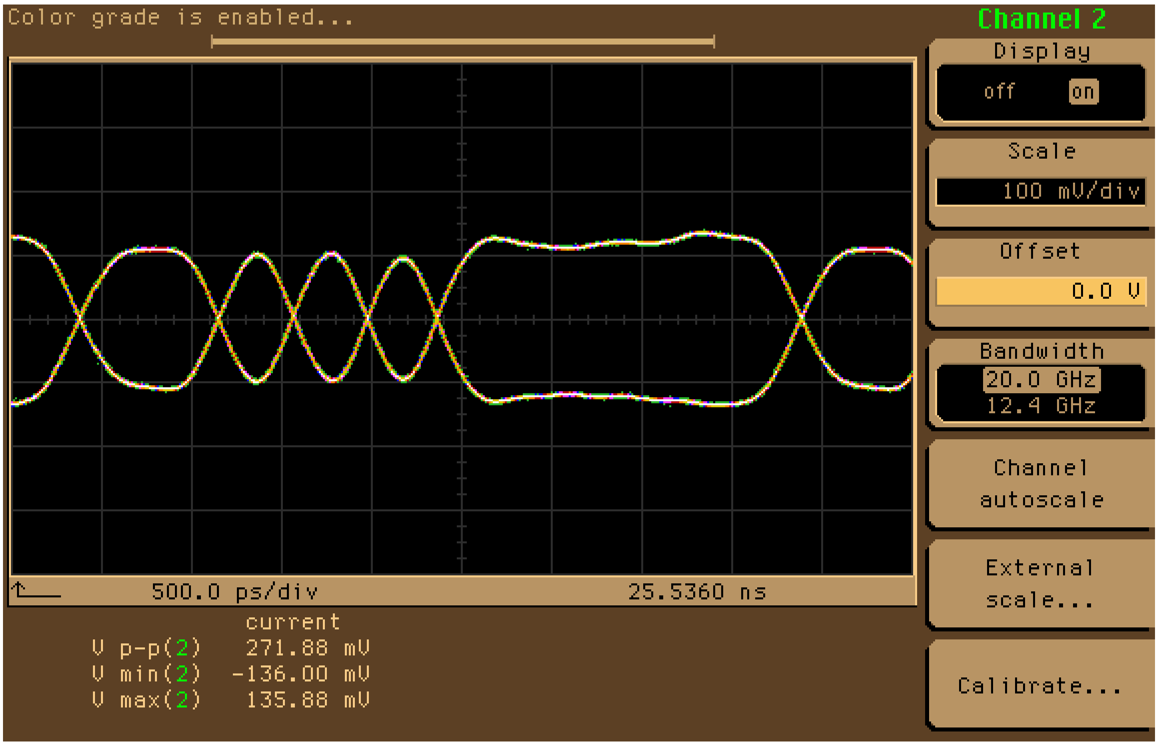
Plot 24

Plot 24 above was the result of driving the Tx through the 10M of cable in PCI mode (low drive). As with the Plot 23 the observed signal is exceptional considering the amount of interconnect involved.



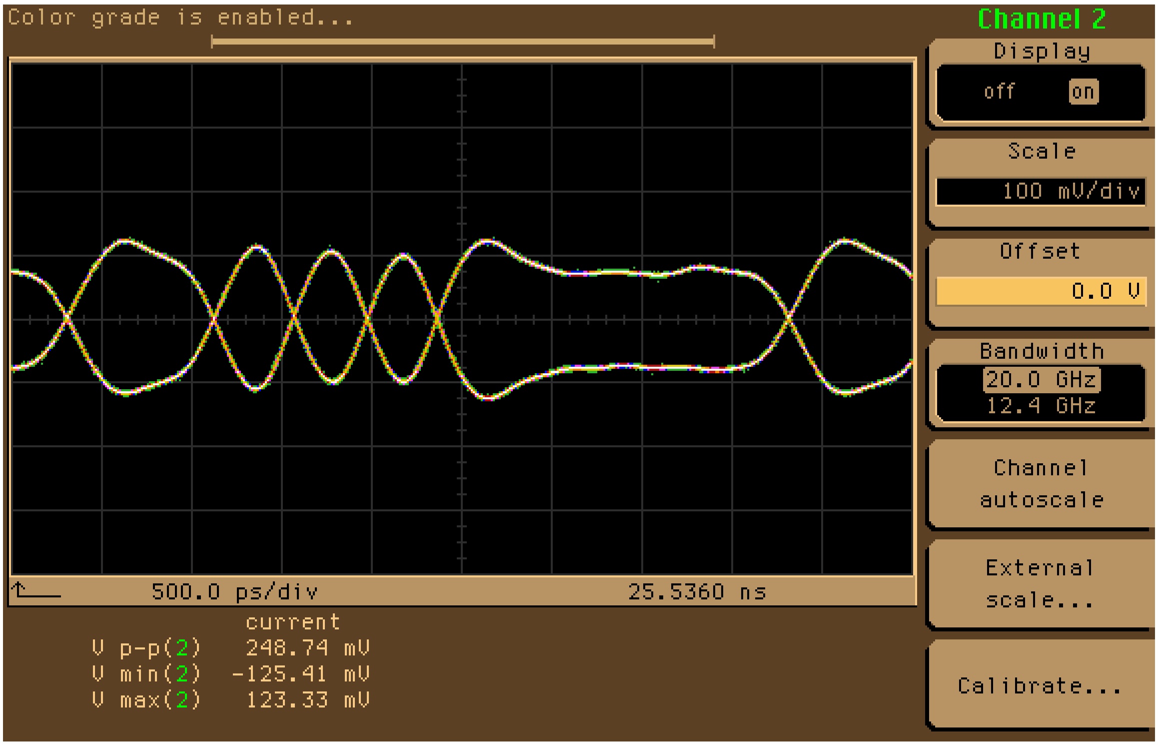
Plot 25

Plot 25 above is the result of switching the Tx cell back to the high drive PCI mode but with the emphasis turned up to the maximum allowable PCI limits.



Plot 26

Plot 26 above shows the Tx cell in PCI low drive mode with the emphasis turned fully on (PCI upper limit). It is quite clear that the driver cell is comfortably driving the 10M of RG58U in the above state.



Plot 27

Finally we put the Tx cell into its full TerraChannel mode with the maximum emphasis and as the result (Plot 27).

All of the above results show excellent performance from the Tx cell, but it should be noted that this is only on a single channel and not in the presence of on chip digital noise.

4.5 Rx testing

The Rx channel was tested using the backend test multiplexer.

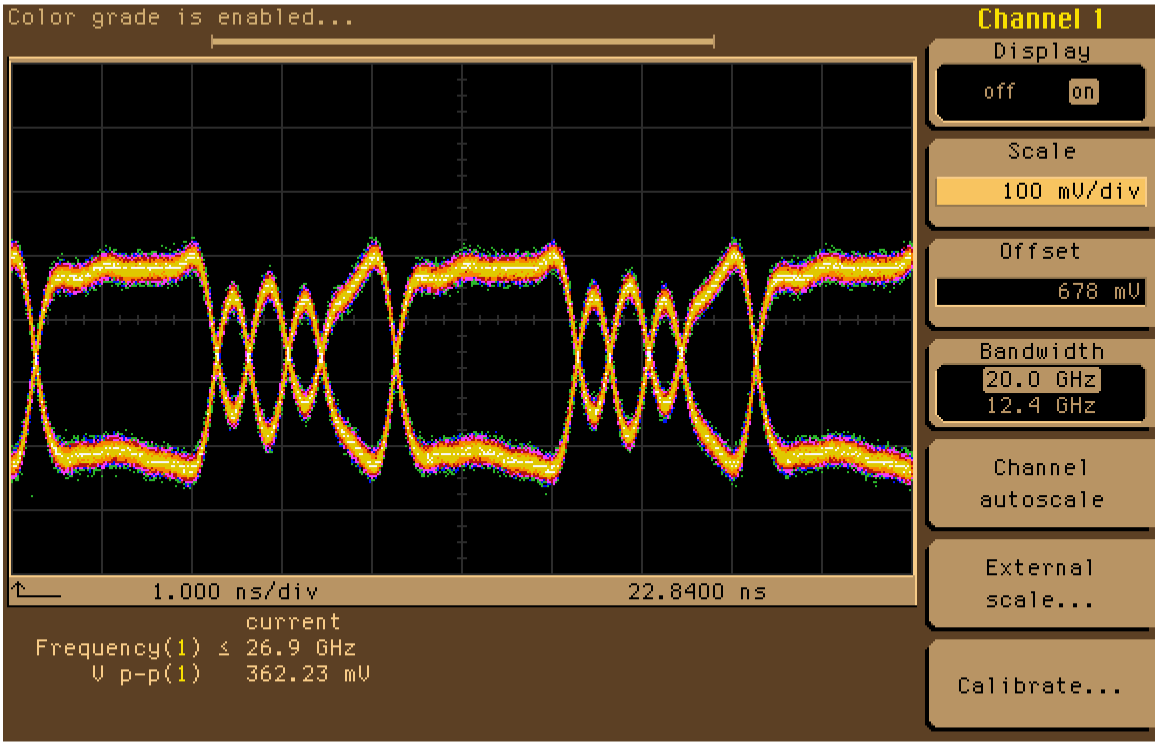
The first test was run simply by using the Tx to generate the K28.5 character and connecting the Tx to Rx via 100 nF AC coupling caps with a few inches of coaxial cable.

The Rx to Tx operation was further confirmed by observation of the Rx_sigdet output from the Rx cell. With the link made from Tx to Rx the sigdet could clearly be seen to be in the high state indicating that a suitable signal had been detected on the Rx inputs above the preset level.

Through the use of the Gore cable assemblies the coupling caps and coaxial cable were replaced with the short 4 inch loop-back cable. To further prove the validity of the Rx cell the Rx was put into the align mode whereby it attempts to lock to the incoming K28.5 character by default. We are able to confirm that the receiver achieved both bit and byte lock by observing a high state on the bit_byte_sync signal. The sigdet was also checked to confirm correct input levels, continually monitoring the sigdet and removing the loopback causes the sigdet to go low.

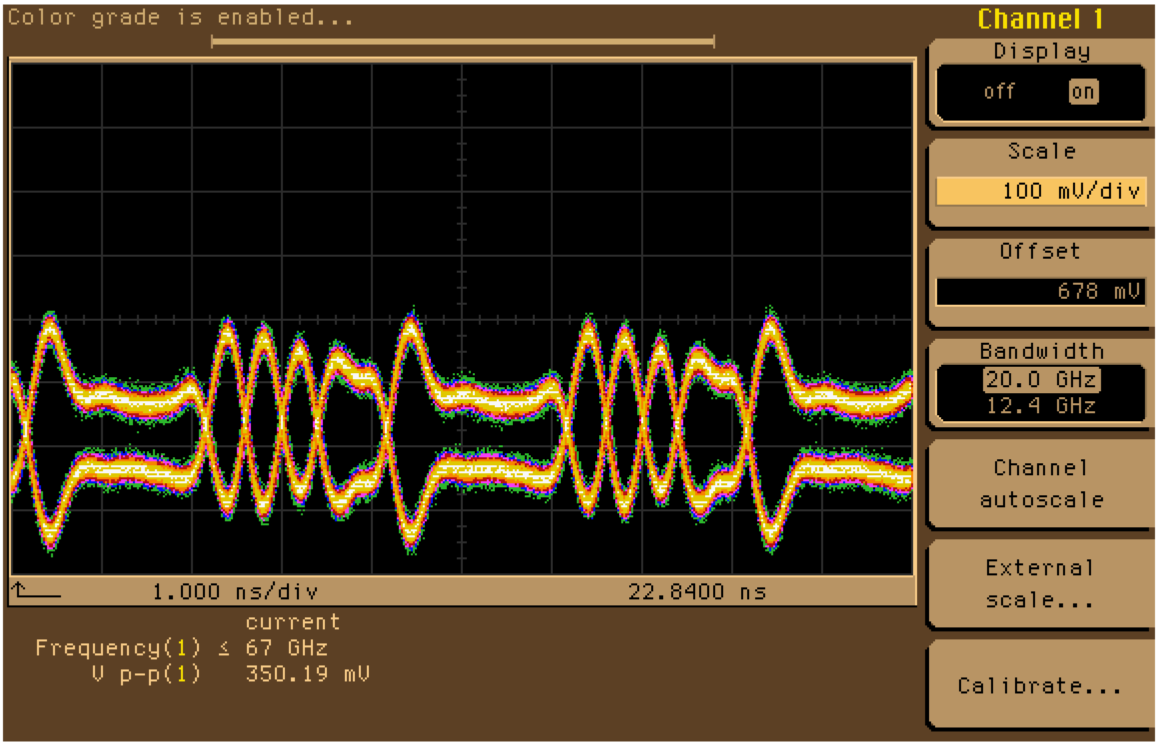
The transceiver was again run through the power up to running to lock states and the inputs into the receiver were captured on the scope via the HF probes. Plots 28 and 29 show the Rx input with the

Tx cell transmitting K28.5 at minimum drive no emphasis, and then finally with full emphasis.



Plot 28

Rx inputs with the Gore loop-back and the Tx cell in Normal drive mode transmitting K28.5



Plot 29

Finally Plot 29 shows Rx inputs with the Gore loop-back and the Tx cell in Normal drive mode, full emphasis transmitting K28.5

In the static reset mode we have the testchip drawing 70mA from the 1.8V supply approximately 126mW.

Putting the common block into running mode we had a drawn current of 240mA. Assuming that the previously measured 70mA is the clock tree and associated logic we have a total drawn current for the common block of 170mA, approximately 305mW.

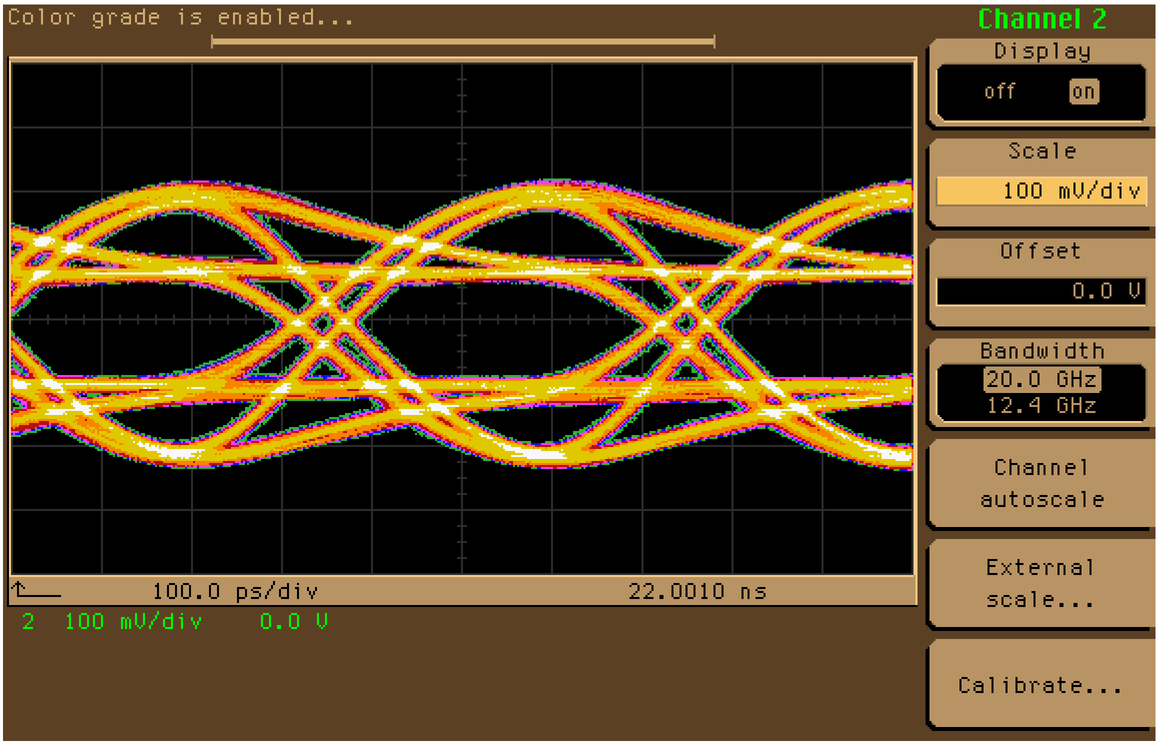
The current drawn by a single transceiver in its active lock state with minimum drive current is 320mA from the 1.8V supply and 26mA from the 2.5V supply. Deducting the 240mA from the 320mA gives us a total drawn current of 80mA for the 1.8V supply, or approximately 145mW. Adding the power from the Driver cell gives a total transceiver power (power in minimum drive mode) of approximately 210mW per channel.

4.6 Bit Error Rate (BER) testing

The initial testing of the new BER checker resulted in the error counter slowly incrementing with the minimum drive set on the transmitter and no pre-emphasis. The pre-emphasis was therefore set to the maximum to see if the transceiver was as resilient to the illegal codes as expected (from the cable test results) with the BER counter being continually monitored. No errors were recorded. To further test the transceiver and gain a quantitative measurement of BER the transceiver was left soak testing BER over the weekend. On checking the counter the next morning we had a reading of ZERO errors on the counter.

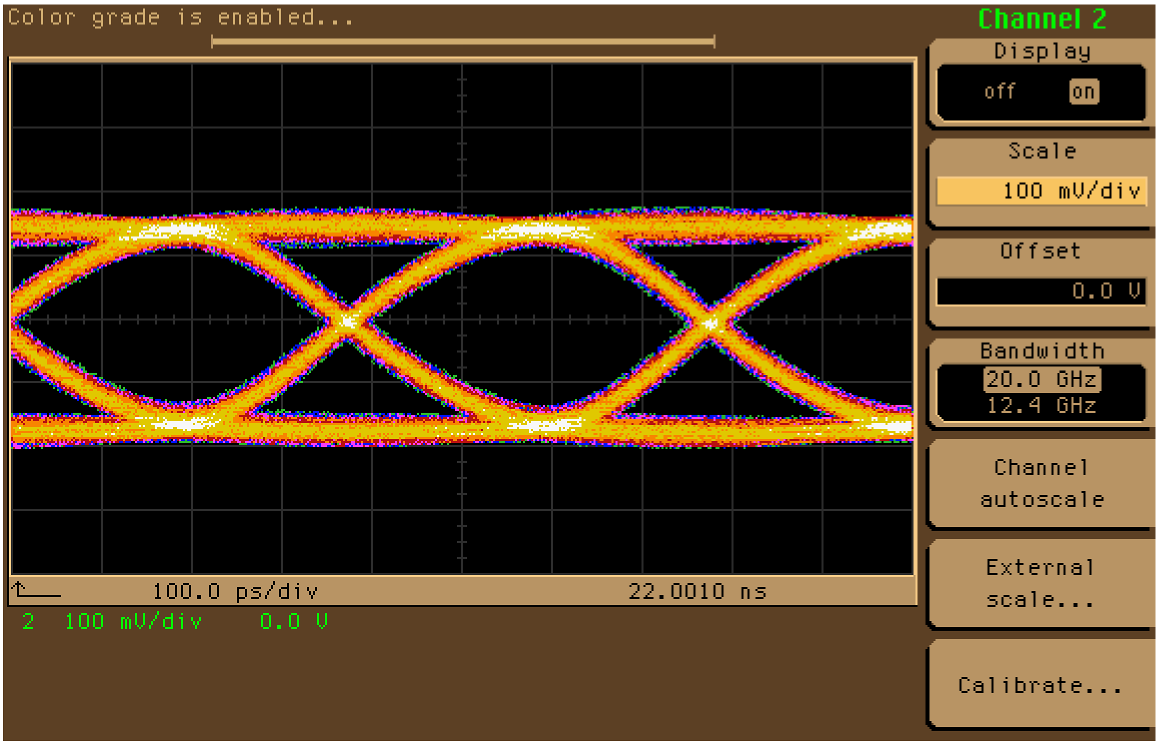
The theoretical number of errors we would expect to see in an hour with a target error rate of 1e-12 is 9 errors; the theoretical number of errors we would expect to see in a day with a target error rate of 1e-14 is 2. Based on the measured results from the 4 day soak test we can be highly confident that the link error rate is better than 1e-12 and probably closer to 1e-14.

Plots 30 and 31 below show the output PRBS stream from the transmitters with the emphasis turned to fully on and with only one bit of compensation can be viewed below.



Plot 30

Plot 30 above shows the PRBS data with pre-emphasis turned fully on.



Plot 31

Plot 31 above shows the PRBS data with the transceiver in TeraChannel mode minimum emphasis.

4.7 Power dissipation summary

A brief summary of the devices tested showed:

- The average power consumption of the Common block at 300mW,
- The average power consumption of the Transceiver at 277mW,
- The average power consumption of the TX Driver cell at 50mW,
- The Yield based on the tested devices at 94%

5 CONCLUSIONS

The extensive testing conducted on the Cronos testchip have shown a very good correlation between the actual transceiver performance and that predicted in the modelling and simulations work. This demonstrates that the chip design workflow can be expected to deliver TeraChannel devices which will perform as expected and will be suitable for the SIVSS application.